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***Wafer Foundry Services***

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## Table of Contents

### Supertex Wafer Foundry

Introduction .....	3
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### Silicon Valley Wafer Fabrication Facility

### Wafer Manufacturing Process Technologies

Services .....	4
Quality and Reliability .....	5
Life Support Policy.....	5
General Information.....	5
Quality Assurance.....	6

### Wafer Manufacturing Process Technologies

Process Technology Overview .....	10
Wafer Manufacturing Processes.....	11
0.6 $\mu$ m CMOS Process .....	12
0.8 $\mu$ m CMOS Process .....	13
1.2 $\mu$ m CMOS Process .....	14
2.0 $\mu$ m N-Well CMOS Process .....	16
2.0 $\mu$ m P-Well CMOS Process .....	18
3.0 $\mu$ m N-Well CMOS Process .....	19
3.0 $\mu$ m P-Well CMOS Process .....	20
4.0 $\mu$ m P-Well CMOS Process (For Analog and Mixed Signal Use) .....	21
5.0 $\mu$ m P-Well CMOS Process (For Analog and Mixed Signal Use) .....	23
CCD Processes.....	24
CMOS CCD Processes.....	25
Rad Hard Process (1.2 $\mu$ m Double Poly, Double Metal).....	26

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**Supertex inc.**

## Supertex Wafer Foundry

### Introduction

### Advanced Solutions for Custom IC Requirements

The Supertex 6-inch submicron wafer fab provides a broad offering of CMOS and CCD technologies as well as Rad Hard capabilities that meet the diverse needs of customers focused on the telecom/networking, imaging, medical and consumer/industrial/computing markets. In addition, the Supertex foundry has the ability to apply our Standard Product technologies such as high voltage CMOS, DMOS and BiCMOS to achieve specific customer product performance requirements.

### Offering Practical and Cost Effective Solutions

These technologies can be modified using our diverse photolithography equipment to support custom needs ranging from 0.5 $\mu$ m feature size and to very large wafer scale charge couple devices (CCDs) and imagers, requiring stitching several chips into one. Our commitment is to partner with our Foundry customers to achieve their product goals.

### Ensuring First-Silicon Success

In addition to our standard processes, our multi-disciplined process engineers provide solutions by modifying our existing processes or developing new processes. Our foundry engineering has a wide range of experience and achievements in semiconductor technology and manufacturing. Working with customers throughout development and production cycles, we establish realistic time lines and provide continuous progress updates to ensure quality solutions on a timely basis.

### Our Goal

The key thrust of our foundry activity is (a) to work closely with our customers to satisfy their IC manufacturing needs, (b) to support their production requirements and (c) to provide guidance and support for future product needs. Supertex can supply tested wafers, dice or provide a complete turnkey solution of tested, packaged ICs.

### History

- Supertex foundry business starts - 1976
- Paradigm, a supplier of advanced memory products, builds 5" fab in early '90s, upgrades it to 6" in 1996
- Supertex purchases fab from Orbit Semiconductor - February 1999
- Acquisition significantly boosts foundry business

### Facility

- ISO 9001 Registered
- 18,000 square feet - 6-inch wafer fab / 6,000 wafer-starts per month
- 9,000 square feet - Class 10 Clean Room
- All Supertex products, both foundry and standard, manufactured here

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## Wafer Manufacturing Capabilities

### Unique Features

- U.S. Owned Submicron CMOS Foundry located in San Jose, California
- Radiation Hardened Capability
- CCD and CMOS Imagers
- Low Temperature Coefficient SiCr Resistor
- Ability to Customize Processes to meet Customer Requirements

### Services

- 6 inch wafer / 6,000 wafer starts per month
- Committed to working closely with customers to achieve their product goals
- A strong, multi-disciplined process engineering team experienced in producing foundry and Supertex standard products
- Market Focus includes: (but not limited to)
  - Imaging IC's (CCD's, CID's, Photo diode Arrays)
  - Medical
  - Military & Hi Rel
  - RAD Hard
  - High Voltage CMOS
  - Analog and Mixed Signal
  - Automotive
- Can supply tested wafers, dice or provide a complete turnkey solution of tested packaged products
- Very large die available by using our P&E 700 projection aligners or with die stitching using our Canon I-line steppers
- MEMS Technologies
- Supertex standard High Voltage and DMOS technologies may be applied to foundry requirements
- Work continuously with customer throughout product evolution cycles
- Design Rules and Spice Models available upon request

## Wafer Manufacturing Process Technologies

### Quality and Reliability

Supertex maintains R & QA programs at critical operations to assure that products are manufactured under a documented and controlled system for consistency in workmanship standards (fit, form, function, and reliability).

The following Standards and Specifications have been integrated into Supertex's manufacturing operations and process control programs:

- ISO 9001 International Standard, Quality Management and Quality System
- FED-STD-209 Clean Room and Work Station Requirements, Controlled Environments
- MIL-HDBK-263 Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment
- MIL-STD-1686 Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment
- MIL-PRF-38535 Microcircuits, General Specification For
- MIL-I-45208 Inspection Systems
- MIL-PRF-19500 Semiconductor Devices, General Specification For
- ASQZ-Z1.4 Sampling Procedures and Tables for Inspection by Attributes
- MIL-STD-750 Test Methods for Semiconductor Devices
- MIL-STD-883 Test Method and Procedures for Microelectronics
- MIL-STD-202 Test Methods for Electronic and Electrical Component Parts
- ANSI-NCSL Z540.1 Calibration System Requirements
- ISO TS16949 Currently in Process of Implementation
- Special Customer Specifications

### Life Support Policy

As a general policy, Supertex, Inc. does not recommend the use of any of its products in any of the following: (a) life support applications where the failure or malfunction of the Supertex product can be reasonably expected to cause failure of the life support device or to significantly affect its safety or effectiveness; or (b) any nuclear facility. Supertex will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement," satisfactory to Supertex, stating that the risks of injury or damage have been minimized, that the customer assumes all such risks, and that the liability of Supertex is adequately covered in the customer's insurance policy.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (for any use), auto transfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, peritoneal dialysis systems, ventilators of all types, infusion pumps, and any other devices designated as "critical" by the FDA. The above are representative examples only and are not intended to be conclusive or exclusive of any other life support device.

Examples of nuclear facility applications are applications in (a) a nuclear reactor; or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing or disposal of fissionable material or waste products thereof.

### General Information

This capabilities brochure has been carefully checked and is believed to be accurate. However, no responsibility is assumed for possible omissions or inaccuracies; specifications are subject to change without notice. Supertex recommends that customers obtain the latest version of the relevant information to establish, prior to ordering, that the information being relied upon is current.

Supertex cannot assume responsibility for customer designed circuits and circuit layouts. Liability of Supertex to circuits it manufactures is limited to replacement of such circuits if they are determined to be defective due to workmanship and not due to misuse or mishandling.

## **Quality Assurance**

The Management of Supertex, Inc. is committed to the continued enhancement of product excellence and service through the dynamics of its Reliability and Quality Assurance System, through the integrity of its people, and through the many professional disciplines engaged in new product development and process innovation.

It is the chartered responsibility of the Reliability and Quality Assurance Director to oversee and ensure enforcement of Supertex's Quality System. A timely review is undertaken to ensure continued development of a Quality System that maintains a competitive stance with the marketplace and meets customer requirements.

### **Primary Job Charter of the QA & R Departments**

**In-Process QC** – The primary responsibilities of the Quality Control Department are to establish and maintain effective controls for monitoring manufacturing processes and equipment; to provide real time feedback of information concerning the state-of-control; and to initiate statistically valid techniques to further improve quality and reliability levels. This concept is used extensively in, but not limited to, the following major Quality Control functions:

- Incoming Raw Materials
- In-process Wafer Fabrication

**Quality Assurance (Standard and Hi-Reliability)** – The primary responsibilities of the Quality Assurance Department are to assure that the delivered product meets workmanship standards imposed for standard or hi-reliability products and/or special customer requirements. This is accomplished through a program of process controls and gate inspections designed so that all devices are properly tested and sampled prior to shipment. Real time feedback, concerning control/inspection data, keeps all relevant personnel fully informed on the quality level of product going through final test operations. Major Quality Assurance functions include:

- Incoming Contract Subassemblies
- Outgoing Wafer Visual Inspection
- Plant Clearance

**Document Control** – The primary responsibilities of the Document Control department are to translate and format internal operating procedures and customer requirements into a system of regulatory written instructions. Document Control functions to ensure documentation integrity by establishing and maintaining procedures for:

- Initiating, revising, approving, distributing, recalling, and archiving documents.

### **Organization**

The Director of Quality Assurance/Quality Control reports directly to executive staff level of Management.

It is the responsibility of the R & QA Director to administer the planning, organization, execution, surveillance, appraisal, corrective action and documentation of Quality Programs. The character, responsibility and authority vested with the R & QA Director will establish the means to attain the necessary quality and reliability objectives in all aspects of manufacturing within the accorded guidelines of this manual.

## Quality programs administered by the R & QA Department support the following functions:

**Operator Training** – Supertex maintains a System of Operator Training and Qualification specific to the nature and complexity of each manufacturing operation, inspection, or test requirement. The basic training approach used by Supertex is supervised on-the-job training assisted by experienced/qualified personnel to provide a “buddy system” of training.

Training is typically performed with the same equipment and tools used in the normal manufacturing environment. The use of training aids, such as films, photographs and demonstrations of equipment and tools, is typical.

Each department manager is responsible for the training and evaluation of the workmanship performance to manufacturing norms.

The R & QA department maintains a system of audits/monitors for evaluating operator’s adherence to specification and quality of workmanship.

**Raw Material Procurement and Qualification** – Supertex maintains a system that ensures economical control and conformance to detailed technical and quality requirements of purchased materials (direct and critical indirect). Material procurement is performed through regulated specifications and drawings. R & QA functions within this system by providing the following services:

- Documented instructions for material evaluation, procedures, flow, workmanship standards, test methods and statistical sampling.
- Incoming inspection of raw materials.
- Identification and segregation of qualified and nonconforming material.
- Vendor qualification and ongoing vendor performance appraisal.
- Feedback of inspection results and informing suppliers of new design changes on raw materials.
- Formal review for disposition of nonconforming materials.

**Equipment Calibration** – Supertex maintains a Calibration System that ensures measurement accuracy of equipment used to determine product workmanship and acceptability.

The Calibration System conforms to ANSI/NCSL Z540-1. Major provisions of the R & QA program are described as follows:

- Qualification of external calibration services.
- Traceability of references to National Institution of Standards and Technology. Identifications of measurement and test equipment (electrical, mechanical, and optical) for type and frequency of calibration.
- Document file certifying equipment calibration and recall history.
- Management report on recall status.
- R & QA audits of equipment calibration (date stickers and recall designation).

**Manufacturing Flow, Inspection, and Test Points** – Supertex maintains Flow Charts that describe the sequential steps of semiconductor processing and associated documentation for Wafer Fabrication. Flow charts are prepared for each product family and associated manufacturing technology.

Flow charts that delineate Fabrication processing are regarded as proprietary and are not available for external dissemination without prior approvals from the foundry customer.

Flow charts for Customer Hi-Reliability Products are documented by a detailed lot traveler which defines all sequential operations, manufacturing inspection points, Customer Source Inspection points, and Quality Assurance product sample acceptance points.

**In-Process Quality Control** – Quality Control is a system of measurement and surveillance. The System is comprised of visual, dimensional, structural, and electrical characterization of material from incoming receipt of raw goods to outgoing finished product. Information obtained provides management with an overview on the state-of-the-process by specifically quantifying position of product yield, quality, and reliability.

Major elements found in Supertex's Quality Control Program are summarized by, but not limited to, the following:

- Environmental monitors (Airborne Particle counts, % RH and temperature).
- Routine Scanning Electron Micrography (SEM) of semiconductor devices.
- Specification compliance audits.
- Random monitor of wafers in-process.
- Electrostatic discharge prevention/monitor.
- Product lot sample qualification at critical manufacturing points.
- Wafer/die electrical sort monitor.
- Quality performance/trend data reporting.
- Return material analysis reporting.
- Monitoring of storage, handling, packaging, and identification of raw materials, of work-in-process, and of finished product.

Product Assurance Inspection – Supertex maintains a system of Product Qualification through inspection and test of finished product prior to customer shipment.

The Quality Assurance department provides inspection based on statistical sampling to ensure that outgoing product quality meets internal workmanship standards and customer procurement requirements.

The following process controls, inspections, tests, and documentation requirements are assured prior to submission of product to Customer Source Inspection and final Outgoing Plant Clearance:

- Test equipment correlation and qualification.
- Monitor manufacturing test operations.
- Ensure conformance of product lots to detailed customer test requirements (electrical, external visual, mechanical).
- Assure proper and complete documentation for each product lot, both in-process and at-plant clearance.

Reliability Assurance – At Supertex the Reliability Concept is introduced at the design phase of all new Supertex standard products. The factors that may affect product reliability are: compatibility of fabrication process, circuit layout and characteristics, assembly process, package materials, and application. Hence, Reliability Engineering is involved in evaluating all critical factors of reliability, starting with the design and first prototype functional circuit. From analysis, modification of design, wafer fabrication, and assembly, process changes can be implemented to enhance the reliability of the product. Approval is given for the release of new product to manufacturing only after the reliability of the product is established as acceptable within standard norms. Upon agreement, Supertex can provide reliability services to the Foundry customers.

## Failure Analysis

- It is the policy of Supertex to perform analysis of defective product and utilize the resulting findings to improve product yield and integrity.
- Reliability Engineering also performs failure analysis in mode and the mechanism of all failures (both from routine reliability tests and customer returns).

## Failure Analysis Support Activities include:

- Qualification of existing products for new applications.
- Customer Qualifications. Reliability is responsible for review and acceptance of all customer requirements. When qualification programs or special testing is required, Reliability designs and implements appropriate test plans and coordinates with customer.
- Failure analysis, in support of In-Process Quality Control monitors, is handled by Reliability through Failure Report Requests. This support includes such services as visual inspection, metalography, thickness measurements, selective etching, and die probing.
- Customer's requests for failure analysis are filled by Reliability, which coordinates all replies to customers and approves all correspondence outside the Company.
- Where Reliability has determined that corrective action is necessary prior to the release of product for shipment, or to proceed further in production processing, a Corrective Action Request is generated by Reliability. No shipment may occur if the integrity of product reliability would be jeopardized.

## **Reporting and Publication of Data**

Qualification test reports are prepared and distributed by Reliability for all certified products and processes which have been formally qualified and released for manufacturing.

Presently, the in-house Reliability Assurance testing is supplemented by testing done at outside Test Laboratories that have been approved by DESC for performing MIL-STD testing.

Supertex reliability data for standard product is published for internal use. Specific reliability information is made available to customers upon request.

Plant Clearance Inspection – Supertex maintains a Final Outgoing Inspection to ensure that all conditions of processing have been satisfied and that support documentation, as specified by contract, is maintained for each shipped lot.

Provisions for the control of shipped product during the Outgoing Plant Clearance Final Acceptance Program are structured to ensure product workmanship guarantees are met.

## Wafer Manufacturing Process Technologies

### Process Technology Overview

Supertex Foundry has processes covering a wide range of technologies. Most processes are available with double poly and double metal layers. The following are some standard processes available for foundry services:

Process Parameters: <i>Technology:</i>		4.0 Micron CMOS	3.0 Micron CMOS (*w/LDD)	2.0 Micron CMOS (*w/LDD)	1.2 Micron CMOS (1 poly)	1.2 Micron CMOS (2 poly)	0.8 Micron CMOS	0.6 Micron CMOS
Well Type		p-Well	n-Well or p-Well	n-Well or p-Well	Twin-Well	Twin-Well	Twin-Well	Twin-Well
Poly Layers		Single/Double	Single/Double	Single/Double	Single	Double	Single/Double	Single/Double
Poly Width/Space (μm)	1st	4.0/3.0	3.0/3.0	2.0/2.5	1.2/1.4	1.2/1.4	0.8/1.0	0.6/0.7
	2nd	4.0/4.0	3.0/3.0	2.0/3.0	NA	1.6/2.2	0.8/1.0	0.6/0.7
Metal Layers		Single/Double	Single/Double	Single/Double	Single/Double	Single/Double	Single/Double /Triple	Single/Double
Metal 1 Width/Space (μm)		4.0/4.0	4.0/3.0	2.5/2.5	2.2/1.2	2.2/1.2	1.4/1.0	0.8/0.8
Metal 2 Width/Space (μm)		6.0/4.0	4.0/4.0	3.0/3.0	2.0/1.6	2.0/1.6	1.4/1.0	0.8/0.9
Metal 3 Width/Space (μm)		NA	NA	3.6/3.0	3.6/3.0	3.6/3.0	1.6/1.4	NA
Contact Width/Space (μm)		3.0/3.0	3.0/3.0	2.0/2.0	1.2/1.4	1.2/1.4	0.8/0.8	0.6/0.6
Via 1 Width/Space (μm)		4.0/4.0	3.0/3.0	2.0/2.5	1.2/1.6	1.2/1.6	1.0/1.0	0.6/0.8
Via 2 Width/Space (μm)		NA	NA	2.0/2.5	2.0/2.0	2.0/2.0	1.2/1.4	NA
Maximum Operating Voltage (V)		15	*12/5.5	*20,*10, 5.5	5.5	5.5	5.5	5.5
Gate Oxide Thickness (Å)		580	500	400	225	225	150/175	130
BVDSSN (Typ.) (V)		21.5	*24/19	15	16	14.5	14	11
BVDSSP (Typ.) (V)		-22	*-18/-17	-15	-15	-14.5	-11	-8

\*Consult factory for LDD option.

## **Wafer Manufacturing Process Technologies**

### **Wafer Manufacturing Processes**

Supertex Foundry has processes covering a wide range of technologies. Most processes are available with double poly and double metal layers. The following are some standard processes available for foundry services:

**0.6 $\mu$ m CMOS Process**

**0.8 $\mu$ m CMOS Process**

**1.2 $\mu$ m CMOS Process**

**2.0 $\mu$ m N-Well CMOS Process**

**2.0 $\mu$ m P-Well CMOS Process**

**3.0 $\mu$ m N-Well CMOS Process**

**3.0 $\mu$ m P-Well CMOS Process**

**4.0 $\mu$ m P-Well CMOS Process**

**5.0 $\mu$ m P-Well CMOS Process**

**CCD Processes**

**CMOS CCD Processes**

**Rad Hard Process**

## 0.6 $\mu$ m CMOS Process

### Standard Features

- Single or double poly
- Double metal
- 5.5V max operating voltage
- Twin well

### Process Technology

- 5x Stepper
- EPI starting material provides latch-up protection
- Double well implant
- LDD for hot electron reliability
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	0.6	$\mu$ m
Gate oxide	130	Å
Inter-poly dielectric	254	Å
Active (width/space)	0.6/1.0	$\mu$ m
Poly 1 (width/space) (Cap Bottom Plate)	0.6/0.7	$\mu$ m
Poly 2 (width/space) (CMOS Gate and Cap Top Plate)	0.6/0.7	$\mu$ m
Contact (width/space)	0.6/0.6	$\mu$ m
Via (width/space)	0.6/0.8	$\mu$ m
Metal 1 (width/space)	0.8/0.8	$\mu$ m
Metal 2 (width/space)	0.8/0.9	$\mu$ m

### Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0 $\mu$ )	0.92	-0.85	V
I <sub>ds</sub>	0.51	-0.27	mA/ $\mu$ m
Gain $\mu$ C (30x30)	110	38	$\mu$ A/V <sup>2</sup>
Body Effect	0.45	0.32	V <sup>1/2</sup>
Sub-threshold slope	90	90	mV/decade
L <sub>eff</sub>	0.48	0.6	$\mu$ m
X <sub>j</sub>	0.27	0.21	$\mu$ m
R <sub>s</sub>	39	100	$\Omega$ /square
R <sub>s</sub> poly	-	24	$\Omega$ /square

## 0.8μm CMOS Process

### Standard Features

- Single or double poly
- Double or triple metal
- 5.5V max operating voltage
- Twin well

### Process Technology

- 5x Stepper
- EPI starting material provides latch-up protection
- Double well implant
- LDD for hot electron reliability
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Process Options

- Non-parasitic N-P-N device
- Native thresholds using implant blocking mask
- Capacitor implant for poly to substrate cap
- 150 or 175Å gate oxide

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	0.8	μm
Gate oxide	150 or 175	Å
Inter-poly dielectric	525	Å
Active (width/space)	0.8/1.6	μm
Poly 1 (width/space)	0.8/1.0 (Cap Bottom Plate)	μm
Poly 2 (width/space)	0.8/1.0 (CMOS Gate and Cap Top Plate)	μm
Contact (width/space)	0.8/0.8	μm
Via 1 (width/space)	1.0/1.0	μm
Via 2 (width/space)	1.2/1.4	μm
Metal 1 (width/space)	1.4/1.0	μm
Metal 2 (width/space)	1.4/1.0	μm
Metal 3 (width/space)	1.6/1.4	μm

### Typical Electrical Parameters (175Å Gate Oxide)

	N-CH	P-CH	Units
Vt(30X2.0μ)	0.87	-0.91	V
IDs	0.32	-0.18	mA/μm
Gain μC (30x30)	91	31	μA/V <sup>2</sup>
Body Effect	0.5	0.35	V <sup>1/2</sup>
Sub-threshold slope	90	90	mV/decade
Leff	0.6	0.7	μm
Xj	0.28	0.28	μm
Rs	46	92	Ω/square

## 1.2 $\mu$ m CMOS Process

### Standard Features

- Single or double poly
- Double Metal
- 5.5V max operating voltage
- Twin Well

### Process Technology

- UT1X or 5x Stepper
- EPI starting material provides latch-up protection
- Double well implant
- LDD for hot electron reliability
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Process Options

- Low threshold for below 5V operation
- High value poly resistor 1k $\Omega$ /square or 25-60k $\Omega$ /square
- Non-parasitic N-P-N device
- Multiple thresholds (Hi/Lo)
- Capacitor implant for poly to substrate cap
- Native thresholds using implant blocking mask
- Triple metal option available

### Process Option Parameters

- Low threshold process:  $V_{tn}$  and  $V_{tp} = 0.5V$  or sum of  $V_t \leq 1.1V$
- Multiple thresholds: Control delta  $V_t$  at 250 to 300mV
- High value poly 2 resistor 1k $\Omega$ /square or 25-60 k $\Omega$ /square
- N-P-N Parameters:

Unit	Value
Rbase	1.6 +/- 0.3 k $\Omega$ /square
Beta	60-250
Vbe	0.65 +/- 0.07V, $I_b = 1\mu A$ , EA = 3.6 x 3.6

### Standard Layout Rules And Process Parameters

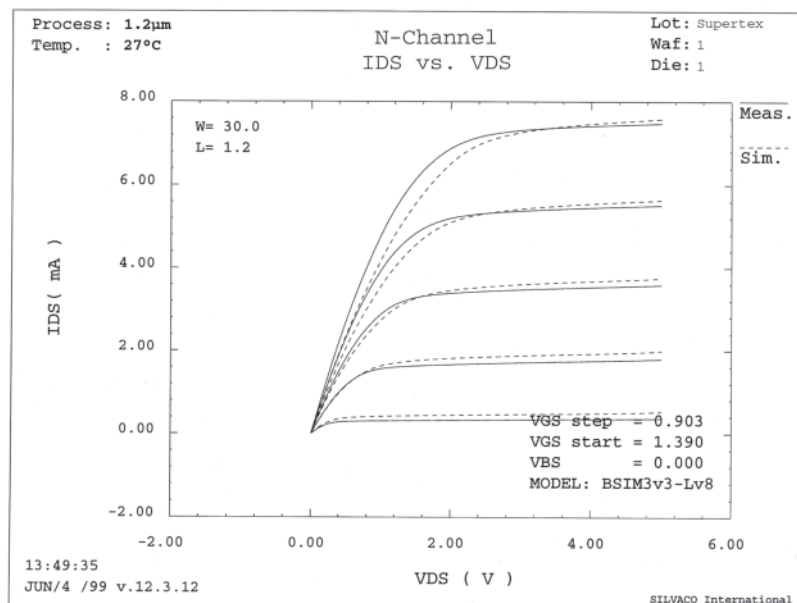
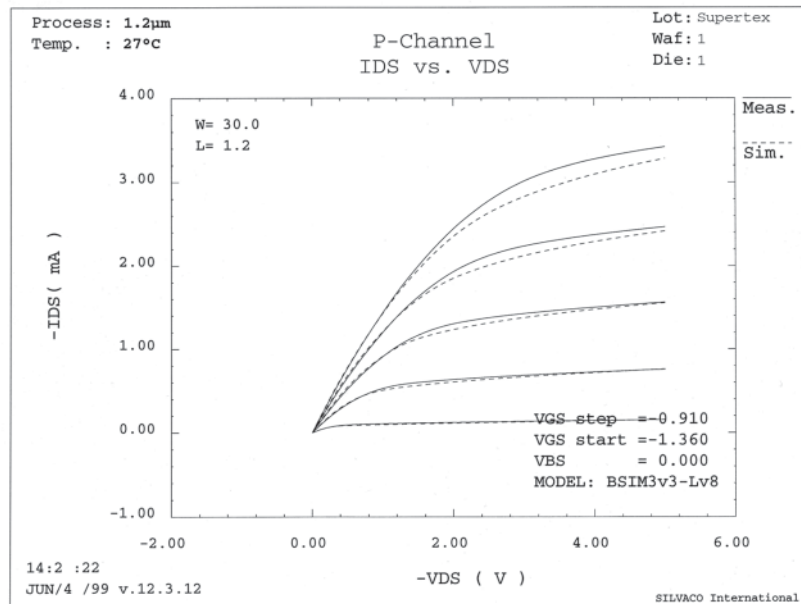
	Value	Units
Min... gate length (N&P)	1.2	$\mu m$
Gate oxide	225	$\text{\AA}$
Inter-poly dielectric	700	$\text{\AA}$
Active (width/space)	2.0/1.2	$\mu m$
Poly 1 (width/space)	1.2/1.4	$\mu m$
Poly 2 (width/space)	1.6/2.2	$\mu m$
Contact (width/space)	1.2/1.4	$\mu m$
Via (width/space)	1.2/1.6	$\mu m$
Metal 1 (width/space)	2.2/1.2	$\mu m$
Metal 2 (width/space)	2.0/1.6	$\mu m$

### Typical Electrical Parameters (Single Poly)

	N-CH	P-CH	Units
$V_t(30 \times 2.0\mu)$	0.83	-0.86	V
$I_{ds}$	0.26	-0.11	$mA/\mu m$
Gain $\mu C(30 \times 30)$	79	29	$\mu A/V^2$
Body Effect	0.7	0.45	$V^{1/2}$
Sub-threshold slope	90	90	mV/decade
$L_{eff}$	0.9	1.1	$\mu m$
$X_j$	0.31	0.39	$\mu m$
$R_s$	38	76	$\Omega$ /square
$R_s$ poly	-	22	$\Omega$ /square

# 1.2 $\mu$ m CMOS Process (cont.)

## Sample Spice Models



## 2.0 $\mu$ m N-Well CMOS Process

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Process Options

- Non-parasitic N-P-N device
- High value poly resistor 1k $\Omega$ /square or 25-60k $\Omega$ /square
- Poly 2 active device allowed
- Native thresholds using implant blocking mask
- Capacitor implant for poly to substrate cap
- 10V or 20V operation with modified layout and LDD
- P & E 700 aligner for large die
- Triple metal option available

### Process Option Parameters

- High value poly 2 resistor 1k $\Omega$ /square or 25-60 k $\Omega$ /square
- N-P-N Parameters:

Unit	Value
Rbase	1.7 +/- 0.3 k $\Omega$ /square
Beta	70-210
Vbe	0.60 +/- 0.07V, Ib = 1 $\mu$ A, EA = 3.6 x 3.6

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	2.0	$\mu$ m
Gate oxide	400	Å
Inter-poly dielectric	700	Å
Active (width/space)	3.0/2.5	$\mu$ m
Poly 1 (width/space)	2.0/2.5	$\mu$ m
Poly 2 (width/space)	2.0/3.0	$\mu$ m
Contact (width/space)	2.0/2.0	$\mu$ m
Via (width/space)	2.0/2.5	$\mu$ m
Metal 1 (width/space)	2.5/2.5	$\mu$ m
Metal 2 (width/space)	3.0/3.0	$\mu$ m

### Typical Electrical Parameters

	N-CH	P-CH	Units
VT(30X2.0 $\mu$ )	0.75	-0.8	V
Ids	0.14	-0.07	mA/ $\mu$ m
Gain $\mu$ C (30x30)	48	14	$\mu$ A/V <sup>2</sup>
Body Effect	0.25	0.42	V <sup>1/2</sup>
Sub-threshold slope	100	100	mV/decade
Leff	1.7	1.6	$\mu$ m
Xj	0.27	0.39	$\mu$ m
Rs	29	60	$\Omega$ /square
Rs poly	-	22	$\Omega$ /square

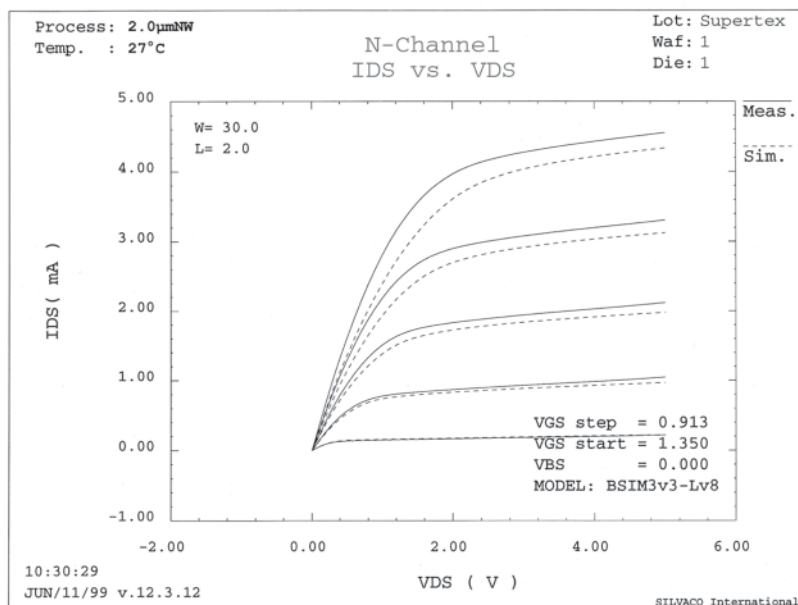
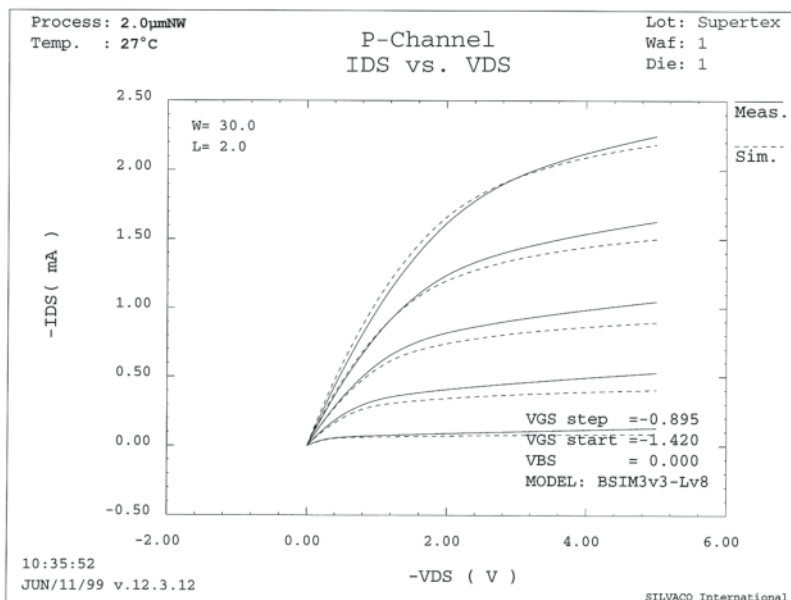
### 10V Operation

#### (With Modified Layout and Spice Models)

- Snap back voltage 15V
- Gated junction breakdown 14V
- Isub max 8 $\mu$ A/ $\mu$ m

## 2.0 $\mu$ m N-Well CMOS Process (cont.)

### Sample Spice Models



## 2.0 $\mu$ m P-Well CMOS Process

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Process Options

- Low threshold for below 5V operation
- High value poly resistor 1k $\Omega$ /square or 25-60k $\Omega$ /square
- Poly 2 active device allowed
- Multiple thresholds with controlled delta
- Capacitor implant for poly to substrate cap
- 10V operation with modified layout and LDD
- P & E 700 aligner for large die
- Native thresholds using implant blocking mask
- Triple metal option available

### Process Option Parameters

- Low threshold process:  $V_{tn}$  and  $V_{tp} = 0.5V$  or Sum of  $V_t \leq 1.1V$
- High value poly 2 resistor 1k $\Omega$ /square or 25-60 k $\Omega$ /square
- LDD N-ch for 10V operation
- Delta  $V_t = 300mV$  on multiple thresholds option

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	2.0	$\mu m$
Gate oxide	400	$\text{\AA}$
Inter-poly dielectric	700	$\text{\AA}$
Active (width/space)	3.0/2.5	$\mu m$
Poly 1 (width/space)	2.0/2.5	$\mu m$
Poly 2 (width/space)	2.0/3.0	$\mu m$
Contact (width/space)	2.0/2.0	$\mu m$
Via (width/space)	2.0/2.5	$\mu m$
Metal 1 (width/space)	2.5/2.5	$\mu m$
Metal 2 (width/space)	3.0/3.0	$\mu m$

### Typical Electrical Parameters

	N-CH	P-CH	Units
$V_t(30 \times 2.0 \mu m)$	0.82	-0.83	V
$I_Ds$	0.14	-0.06	$mA/\mu m$
Gain $\mu C(30 \times 30)$	46	14	$\mu A/V^2$
Body Effect	0.25	0.45	$V^{1/2}$
Sub-threshold slope	100	100	$mV/decade$
$L_{eff}$	1.7	1.6	$\mu m$
$X_j$	0.35	0.5	$\mu m$
$R_s$	18	70	$\Omega/square$
$R_s$ poly	-	28	$\Omega/square$

## 3.0µm N-Well CMOS Process

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection

### Process Options

- Poly 2 (Cap Top Plate)
- Isolated N-P-N
- 12V max operation with N-LDD
- Low TC SiCr Resistor
- P & E 700 aligner for large die

### Process Option Parameters

- N-LDD N-ch for 10V operation, (12V maximum)  
Min. L=4µm (High voltage device has lower drive due to increase in SD resistance. Contact factory for details.)
- Low temperature coefficient SiCr resistor:  
500±100Ω/square
- N-P-N parameters:

Unit	Value
Beta	180
Early Voltage	50V min..
BVceo	25V min...
BVebo	8.2V

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	3.0	µm
Gate oxide	500	Å
Inter-poly dielectric	700	Å
Active (width/space)	4.0/3.0	µm
Poly 1 (width/space)	3.0/3.0	µm
Poly 2 (width/space)	3.0/3.0	µm
Contact (width/space)	3.0/3.0	µm
Via (width/space)	3.0/3.0	µm
Metal 1 (width/space)	4.0/3.0	µm
Metal 2 (width/space)	4.0/4.0	µm

### Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0µ)	0.8	-0.8	V
Ids	0.09	-0.045	mA/µm
Gain µC (30x30)	42	14	µA/V <sup>2</sup>
Body Effect	0.3	0.42	V <sup>1/2</sup>
Sub-threshold slope	100	100	mV/decade
Leff	2.5	2.0	µm
Xj	0.35	0.62	µm
Rs	27	41	Ω/square
Rs poly1	20	27	Ω/square
Rs poly2	28	NA	Ω/square

## 3.0 $\mu$ m P-Well CMOS Process

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection

### Process Options

- Low threshold for below 5V operation  
( $V_{tn}$  and  $V_{tp} = 0.5V$  or sum of  $V_T < 1.2V$ )
- High value poly resistor 1-2 or 25-60 k $\Omega$ /square
- Poly 2 (Cap Top Plate)
- Capacitor implant for poly to substrate cap
- 10V operation with modified layout and LDD
- Low temperature coefficient SiCr resistor  
(500 $\pm$ 100 $\Omega$ K)
- P & E 700 aligner for large die

### Process Option Parameters

- N-LDD N-ch for 10V operation. (High voltage device has lower drive due to increase in SD resistance. Contact factory for details.)
- Low temperature coefficient SiCr resistor:  
500 $\pm$ 100 $\Omega$ /square

### Standard Layout Rules And Process Parameters

	Value	Units
Min... gate length (N&P)	3.0	$\mu$ m
Gate oxide	500	$\text{\AA}$
Inter-poly dielectric	700	$\text{\AA}$
Active (width/space)	4.0/3.0	$\mu$ m
Poly 1 (width/space)	3.0/3.0	$\mu$ m
Poly 2 (width/space)	3.0/3.0	$\mu$ m
Contact (width/space)	3.0/3.0	$\mu$ m
Via (width/space)	3.0/3.0	$\mu$ m
Metal 1 (width/space)	4.0/3.0	$\mu$ m
Metal 2 (width/space)	4.0/4.0	$\mu$ m

### Typical Electrical Parameters

	N-CH	P-CH	Units
$V_t(30 \times 2.0 \mu)$	0.95	-0.7	V
$I_{ds}$	0.07	-0.04	mA/ $\mu$ m
Gain $\mu C(30 \times 30)$	45	16	$\mu A/V^2$
Body Effect	0.8	0.32	$V^{1/2}$
Sub-threshold slope	100	100	mV/decade
$L_{eff}$	1.7	2.0	$\mu$ m
$X_j$	0.8	0.6	$\mu$ m
$R_s$	16	49	$\Omega$ /square
$R_s$ poly1	20	NA	$\Omega$ /square

## 4.0μm P-Well CMOS Process (For Analog and Mixed Signal Use)

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection
- Double diffused N drain and source

### Process Options

- Low threshold for below 5V operation
- Capacitor implant for poly to substrate cap
- P & E 700 aligner for large die

### Process Option Parameters

- Low threshold process:  $V_{tn}$  and  $V_{tp} = 0.5V$  or sum of  $V_T \leq 1.1V$

### Standard Layout Rules And Process Parameters

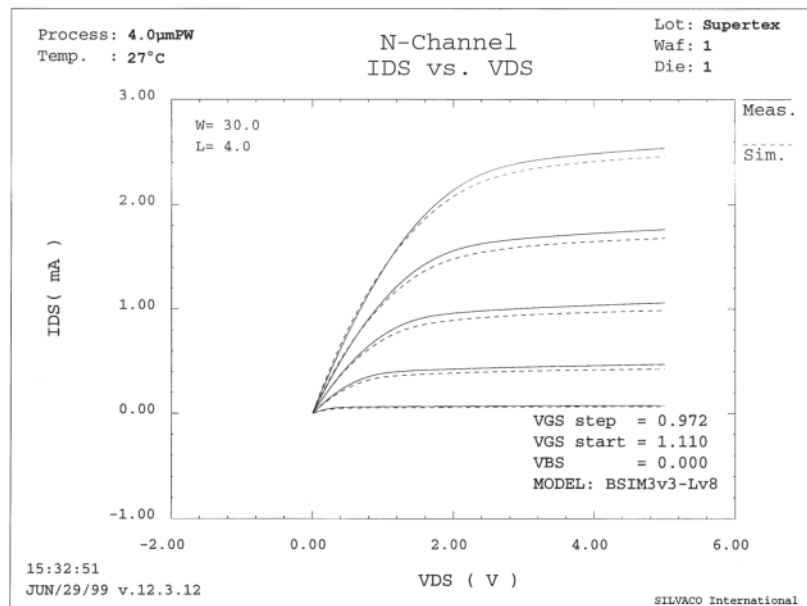
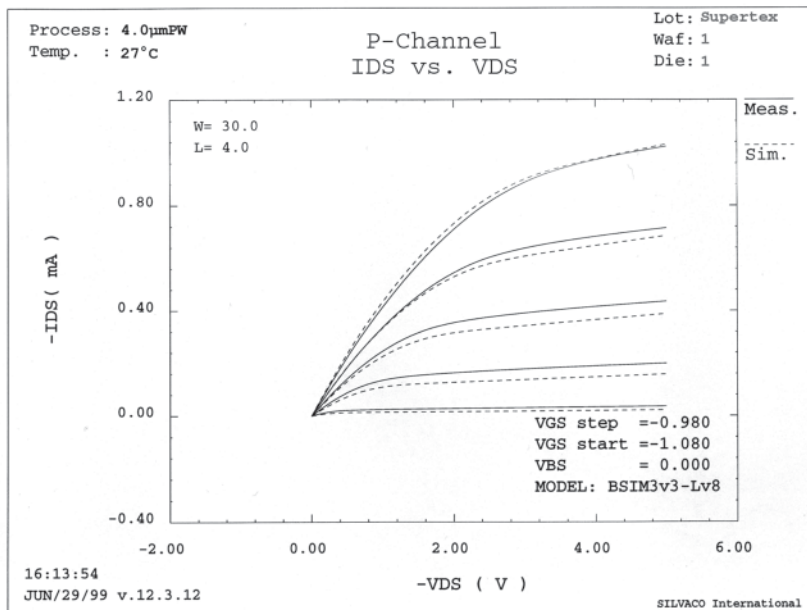
	Value	Units
Min... gate length (N&P)	4.0	μm
Gate oxide	580	Å
Inter-poly dielectric	700	Å
Active (width/space)	4.0/4.0	μm
Poly 1 (width/space)	4.0/3.0	μm
Poly 2 (width/space)	4.0/4.0	μm
Contact (width/space)	3.0/3.0	μm
Via (width/space)	4.0/4.0	μm
Metal 1 (width/space)	4.0/4.0	μm
Metal 2 (width/space)	6.0/4.0	μm

### Typical Electrical Parameters

	N-CH	P-CH	Units
$V_t(30 \times 2.0 \mu)$	0.73	-0.73	V
$I_{ds}$	0.07	-0.03	mA/μm
Gain μC (30x30)	35	12	μA/V <sup>2</sup>
Body Effect	1.1	0.6	V <sup>1/2</sup>
$L_{eff}$	2.5	2.7	μm
$X_j$	0.9	0.7	μm
$R_s$	24	69	Ω/square
$R_s$ poly	-	21	Ω/square

## 4.0 $\mu$ m P-Well CMOS Process (cont.) (For Analog and Mixed Signal Use)

### Sample Spice Models, (Low Threshold Option)



## 5.0μm P-Well CMOS Process (For Analog and Mixed Signal Use)

### Standard Features

- Single or double poly
- Single or double metal
- 15V max operating voltage

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection
- Capacitor implant for poly to substrate cap

### Process Options

- Low threshold process:  $V_{tn}$  and  $V_{tp} = 0.5V$  or sum of  $V_t \leq 1.1V$
- P & E 700 aligner for large die

### Standard Layout Rules and Process Parameters

	Value	Units
Min... gate length (N&P)	5.0	μm
Gate oxide	900	Å
Inter-poly dielectric	700-1000	Å
Active (width/space)	5.0/5.0	μm
Poly 1 (width/space)	5.0/5.0	μm
Poly 2 (width/space)	5.0/5.0	μm
Contact (width/space)	5.0/5.0	μm
Via (width/space)	5.0/5.0	μm
Metal 1 (width/space)	5.0/5.0	μm
Metal 2 (width/space)	5.0/5.0	μm

### Typical Electrical Parameters

	N-CH	P-CH	Units
$V_t(30 \times 2.0 \mu)$	0.8	-0.8	V
$I_{ds}$	0.04	-0.02	mA/μm
Gain $\mu C$ (30x30)	24	8	μA/V <sup>2</sup>
Body Effect	1.0	0.5	V <sup>1/2</sup>
$L_{eff}$	2.5	2.9	μm
$X_j$	1.6	1.3	μm
$R_s$	15	37	Ω/square
$R_s$ poly1	14	17	Ω/square
$R_s$ poly2	22	NA	Ω/square

## CCD Processes

### IMAGERS Standard Features

- P & E 700 aligner for large die
- Stitching available on UT1X or Canon 5X
- EPI
- N-Channel
- 3 poly
- Oxide/Nitride gate dielectric
- Two or three metals (last metal as shield)
- Surface or buried channel

### CCD Process Parameters

	Value	Units
Active (width/space)	3.0/4.0	μm
Poly 1 (width/space)	3.0/2.5	μm
Poly 2 (width/space)	3.0/3.0	μm
Poly 3 (width/space)	3.0/3.0	μm
Contact (width/space)	2.0	μm
Metal 1 (width/space)	4.0/5.0	μm
Metal 2 (width/space)	5.0/6.0	μm

### Process Parameters

	Value	Units
Gate dielectric	500 oxide/500 nitride	Å
Inter poly dielectric	1700-3000	Å
Channel potentials	5-15 customized	V
CCD transfer efficiency	5 9's	
Dark current	< 1 nA/square centimeter	

## CMOS CCD Processes

### 1.2 $\mu$ m CMOS CCD Process

- Integration of CCD elements into a 1.2 $\mu$ m N-well process
- 2 poly, 2 metal
- CCD elements in 5E14/cc p-substrate, may be customized
- Poly 1 is CCD gate electrode and bottom plate of CMOS capacitor only
- Poly 2 is CCD gate electrode and CMOS gate and capacitor top plate
- CCD gate dielectric is oxide/nitride sandwich
- CCD channel potential customized

### CCD Process Parameters

	Value	Units
Poly 1 and poly 2 gate dielectric (oxide/nitride)	325/450	Å
Implant poly channel potential	1.5-2.5 or customized	V
Barrier height between poly 1 and 2 electrodes	1.0-1.5 or customized	V
CCD Inter-poly thickness	900	Å
CCD Transfer efficiency	4 9's minimum	

### CMOS Process and Electrical Parameters

- Refer to our 1.2 $\mu$ m CMOS process

## Rad Hard Process 1.2 $\mu$ m Double Poly, Double Metal

### Standard Features

- Single or double poly
- Single or double metal
- 5.5V max operating voltage
- Twin Well

### Process Technology

- UT1X Stepper
- EPI starting material provides latch-up protection
- Degenerate P-channel stop for N-channel devices
- 225Å gate ox
- Substrate cap implant
- Double poly capacitor
- LDD for hot electron reliability
- Sandwich metal for electromigration
- Titanium nitride barrier metal

### Typical Electrical Parameters for 1.2 $\mu$ m Rad Hard Process (Room Temperature)

	N-CH	P-CH	Units
Vt(30X1.2 $\mu$ )	0.70	-0.72	V
Ids	0.20	-0.09	mA/ $\mu$ m
Gain $\mu$ C (30x30)	66	19	$\mu$ A/V <sup>2</sup>
Body Effect	0.60	0.35	V <sup>1/2</sup>
Sub-threshold slope	90	90	mV/decade
Leff	0.9	1.1	$\mu$ m
Xj	0.3	0.3	$\mu$ m
Rs	31	62	$\Omega$ /square
Rs poly	21	20	$\Omega$ /square

### Rad Hard Parameters

- Vt shift at 250kRad at 78K 0.9 to 1.4V (max)

**Notes:**

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## Notes: