

5.0 μ m P-Well CMOS Process (For Analog and Mixed Signal Use)

Standard Features

- ❖ PE aligner, UTIX
- ❖ Single or double poly
- ❖ Single or double metal
- ❖ 15V max operating voltage

Process Technology

- ❖ EPI starting material provides latch-up protection
- ❖ Capacitor implant for poly to substrate cap

Process Options

- ❖ Low threshold process: V_{tn} and $V_{tp}=0.5V$
or $\text{Sum of } V_t \leq 1.1V$

Standard Layout Rules and Process Parameters

	Value	Units
Min gate length (N & P)	5.0	μm
Gate oxide	900	\AA
Inter-poly oxide	700 – 1000	\AA
Active (width/space)	5.0/5.0	μm
Poly 1 (width/space)	5.0/5.0	μm
Poly 2 (width/space)	5.0/5.0	μm
Contact (width/space)	5.0/5.0	μm
Via (width/space)	5.0/5.0	μm
Metal 1 (width/space)	5.0/5.0	μm
Metal 2 (width/space)	5.0/5.0	μm

Typical Electrical Parameters

	N-CH	P-CH	Units
$V_t(30X4.0\mu)$	0.8	-0.8	V
$I_{ds}(3.0X4.0\mu)$	0.04	-0.02	mA/ μm
Gain μC (30X30)	24	8	$\mu\text{A}/V^2$
Body Effect	1.0	0.5	$V^{1/2}$
L_{eff}	2.5	2.9	μm
X_j	1.6	1.3	μm
R_s	15	37	Ω/square
R_s poly1	14	17	Ω/square
R_s poly2	22	—	Ω/square