Supertex inc.
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3.0µm P-Well CMOS Process

Standard Features

- UTIX Stepper
- Single or double poly
- Single or double metal
- 5.5V max operating voltage

Process Technology

- EPI starting material provides latch-up protection

Process Options

- Low threshold for below 5V operation (V_{tn} and V_{tp} = 0.5V or sum of V_t < 1.2V)
- High value poly resistor 1-2 or 25-60 kΩ/square
- Poly 2 (Cap Top Plate)
- Capacitor implant for poly to substrate cap
- 10V operation with modified layout and N-Ldd
- Low temperature coefficient SiCr resistor (500±100ΩK)
- P & E 760 aligner for large die

Standard Layout Rules and Process Parameters

	Value	Units
Min gate length (N&P)	3.0	µm
Gate oxide	500	Å
Inter-poly dielectric	700	Å
Active (width/space)	4.0/3.0	µm
Poly 1 (width/space)	3.0/3.0	µm
Poly 2 (width/space)	3.0/3.0	µm
Contact (width/space)	3.0/3.0	µm
Via (width/space)	3.0/3.0	µm
Metal 1 (width/space)	4.0/3.0	µm
Metal 2 (width/space)	4.0/4.0	µm

Process Option Parameters

- Low threshold process: Vtn and Vtp = 0.5V or sum of Vt < 1.2V
- High value poly 2 resistor 1-2 or 25-60 kΩ/square
- N-Ldd N-ch for 10V operation, (12V maximum) Min L=4µm (High voltage device has lower drive due to increase in SD resistance. Contact factory for details.)
- Low TC SiCr resistor: 500+/-100 Ω/square

Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0µ)	0.95	-0.70	V
Ids	0.07	-0.04	mA/µm
Gain µC (30X30)	45	16	$\mu A/V^2$
Body Effect	0.8	0.32	$V^{1/2}$
Sub-threshold slope	100	100	mV/decade
Leff	1.7	2.0	µm
Xj	0.8	0.6	µm
Rs	16	49	Ω/square
Rs poly1	11	—	Ω/square

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