Supertex inc.
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3.0µm N-Well CMOS Process

Standard Features

- UTIX Stepper
- Single or double poly
- Single or double metal
- 5.5V max operating voltage

Process Technology

- EPI starting material provides latch-up protection

Process Options

- Poly 2 (Cap Top Plate)
- Isolated N-P-N
- 12V max operation with N-Ldd
- Low TC SiCr Resistor
- P & E 760 aligner for large die

Standard Layout Rules and Process Parameters

	Value	Units
Min gate length (N&P)	3.0	µm
Gate oxide	500	Å
Inter-poly dielectric	700	Å
Active (width/space)	4.0/3.0	µm
Poly 1 (width/space)	3.0/3.0	µm
Poly 2 (width/space)	3.0/3.0	µm
Contact (width/space)	3.0/3.0	µm
Via (width/space)	3.0/3.0	µm
Metal 1 (width/space)	4.0/3.0	µm
Metal 2 (width/space)	4.0/4.0	µm

Process Option Parameters

- N-ldd N-ch for 10V operation, (12V maximum) Min L=4µm (High voltage device has lower drive due to increase in SD resistance. Contact factory for details.)
- Low TC SiCr resistor: 500+/-100 Ω/square
- N-P-N parameters:

Unit	Value
Beta	180
Early Voltage	50V min
BVceo	25V min
BVebo	8.2V

Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0µ)	0.8	-0.8	V
Ids	0.09	-0.045	mA/µm
Gain µC (30X30)	42	14	$\mu A/V^2$
Body Effect	0.3	0.42	$V^{1/2}$
Sub-threshold slope	100	100	mV/decade
Leff	2.5	2.0	µm
Xj	0.35	0.62	µm
Rs	27	41	Ω/square
Rs poly1	20	27	Ω/square
Rs poly2	28	—	Ω/square

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