

2.0 μ m P-Well CMOS Process

Standard Features

- ❖ UT1X Stepper
- ❖ Single or double poly
- ❖ Single or double metal
- ❖ 5.5V max operating voltage

Process Technology

- ❖ EPI starting material provides latch-up protection
- ❖ Titanium nitride barrier metal

Process Options

- ❖ Low threshold for below 5V operation
- ❖ High value poly resistor 1k Ω /square or 25-60 k Ω /square
- ❖ Poly 2 active device allowed
- ❖ Multiple thresholds with controlled delta
- ❖ Capacitor implant for poly to substrate cap
- ❖ 10V operation with modified layout and Ldd
- ❖ P & E 760 aligner for large die
- ❖ Native thresholds using implant blocking mast
- ❖ Triple metal option available

Process Option Parameters

- ❖ Low threshold process: Vtn and Vtp=0.5V or Sum of Vt \leq 1.1V
- ❖ High value poly 2 resistor 1k Ω /square or 25-60 k Ω /square
- ❖ Ldd N-ch for 10V operation
- ❖ Delta Vt=300mV on multiple thresholds option

Standard Layout Rules and Process Parameters

	Value	Units
Min gate length (N&P)	2.0	μ m
Gate oxide	400	Å
Interpoly oxide	700	Å
Active (width/space)	3.0/2.5	μ m
Poly 1 (width/space)	2.0/2.5	μ m
Poly 2 (width/space)	2.0/3.0	μ m
Contact (width/space)	2.0/2.0	μ m
Via (width/space)	2.0/2.5	μ m
Metal 1 (width/space)	2.5/2.5	μ m
Metal 2 (width/space)	3.0/3.0	μ m

Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0 μ)	0.82	-0.83	V
Ids	0.14	-0.60	mA/ μ m
Gain μ C (30X30)	46	14	μ A/V ²
Body Effect	0.25	0.45	V ^{1/2}
Sub-threshold slope	100	100	mV/decade
Leff	1.7	1.6	μ m
Xj	0.35	0.5	μ m
Rs	18	70	Ω /square
Rs poly	—	21	Ω /square