

## 2.0 $\mu$ m N-Well CMOS Process

### Standard Feature

- ❖ UT1X Stepper
- ❖ Single or double poly
- ❖ Single or double metal
- ❖ 5.5V max operating voltage

### Process Technology

- ❖ EPI starting material provides latch-up protection
- ❖ Titanium nitride barrier metal

### Process Options

- ❖ Non-parasitic N-P-N device in N-well
- ❖ High value poly resistor 1k $\Omega$ /square or 25-60 k $\Omega$ /square
- ❖ Poly 2 active device allowed
- ❖ Native thresholds using implant blocking mask
- ❖ Capacitor implant for poly to substrate cap
- ❖ 10V or 20V operation with modified layout and Ldd
- ❖ P & E 760 aligner for large die
- ❖ Triple metal option available

### Process Option Parameters

- ❖ High value poly 2 resistor 1k $\Omega$ /square or 25-60 k $\Omega$ /square
- ❖ N-P-N

Unit	Value
Rbase	1.7 +/-0.3 k $\Omega$ /square
Beta	70-210
Vbe	0.60+/-0.07 volt, Ib=1 $\mu$ A, EA=3.6 X 3.6

### Standard Layout Rules and Process Parameters

	Value	Units
Min gate length (N&P)	2.0	$\mu$ m
Gate oxide	400	Å
Interpoly oxide	700	Å
Active (width/space)	3.0/2.5	$\mu$ m
Poly 1 (width/space)	2.0/2.5	$\mu$ m
Poly 2 (width/space)	2.0/3.0	$\mu$ m
Contact (width/space)	2.0/2.0	$\mu$ m
Via (width/space)	2.0/2.5	$\mu$ m
Metal 1 (width/space)	2.5/2.5	$\mu$ m
Metal 2 (width/space)	3.0/3.0	$\mu$ m

### 10V Operation (With Modified Layout and Spice Models)

- ❖ Snapback Voltage 15V
- ❖ Gated Junction Breakdown 14V
- ❖ Isub max 8 $\mu$ A/W

### Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X2.0 $\mu$ )	0.75	-0.85	V
Ids	0.14	-0.07	mA/ $\mu$ m
Gain $\mu$ C (30X30)	48	14	$\mu$ A/V <sup>2</sup>
Body Effect	0.25	0.45	V <sup>1/2</sup>
Sub-threshold slope	100	100	mV/decade
Leff	1.7	1.6	$\mu$ m
Xj	0.27	0.39	$\mu$ m
Rs	29	60	$\Omega$ /square
Rs poly	—	28	$\Omega$ /square

## 2.0 $\mu$ m N-Well CMOS Process, continued

### Sample Spice Models

