

1.2 μ m CMOS Process

Standard Features

- ❖ UT1X Stepper
- ❖ Single or double poly
- ❖ Single or double metal
- ❖ 5.5V max. operating voltage
- ❖ Twin well (N or P type substrate)

Process Technology

- ❖ EPI starting material provides latch-up protection
- ❖ Double well implant
- ❖ Ldd for hot electron reliability
- ❖ Titanium nitride barrier metal

Process Options

- ❖ Low threshold for less than 5V operation
- ❖ Multiple thresholds (Hi/Lo)
- ❖ Non-parasitic N-P-N device
- ❖ High value poly resistor 1k Ω /square or 25-60 k Ω /square
- ❖ Capacitor implant for poly to substrate cap
- ❖ Native thresholds using implant blocking mask
- ❖ Triple metal option available

Process Option Parameters

- ❖ Low threshold process: V_{tn} and $V_{tp}=0.5V$ or $\text{Sum of } V_t \leq 1.1V$
- ❖ Multiple thresholds: Control ΔV_t at 250 to 300mV
- ❖ High value poly 2 resistor 1k Ω /square or 25-60 k Ω /square
- ❖ N-P-N

Unit	Value
Rbase	1.6 +/-0.3 k Ω /square
Beta	60-250
Vbe	0.65 +/-0.07 V, $I_b=1\mu A$, $E_A=3.6 \times 3.6$

Standard Layout Rules and Process Parameters

	Values	Units
Min gate length (N&P)	1.2	μm
Gate oxide	225	\AA
Inter-poly oxide	700	\AA
Active (width/space)	2.0/1.2	μm
Poly 1 (width/space)	1.2/1.4	μm
Poly 2 (width/space)	1.6/2.2	μm
Contact (width/space)	1.2/1.4	μm
Via (width/space)	1.2/1.6	μm
Metal 1 (width/space)	2.2/1.2	μm
Metal 2 (width/space)	2.0/1.6	μm

Typical Electrical Parameters (Single Poly)

	N-CH	P-CH	Units
$V_t(30 \times 1.2\mu)$	0.83	-0.86	V
I_{ds}	0.26	-0.11	mA/ μm
Gain $\mu C(30 \times 30)$	79	29	$\mu A/V^2$
Body Effect	0.7	0.45	$V^{1/2}$
Sub-threshold slope	90	90	mV/decade
L_{eff}	0.9	1.1	μm
X_j	0.31	0.39	μm
R_s	38	76	Ω /square
R_s poly	—	22	Ω /square

1.2 μ m CMOS Process, continued

Sample Spice Models

