Supertex inc.
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0.8µm CMOS Process

Standard Features

- Single or double poly
- Double or triple metal
- 5.5V max operating voltage
- Twin well

Process Technology

- 5X Stepper
- EPI starting material provides latch-up protection
- Double well implant
- Ldd for hot electron reliability
- Sandwich metal for e-m
- Titanium nitride barrier metal

Process Options

- Native thresholds using implant blocking mask
- Capacitor implant for poly to substrate capacitor
- 150 or 175 Å gate oxide

Standard Layout Rules and Process Parameters

	Values	Units
Min gate length (N&P)	0.8	µm
Gate oxide	150 or175	Å
Inter-poly dielectric (oxide equiv.)	525	Å
Active (width/space)	0.8/1.6	µm
Poly 1 (width/space)	0.8/1.0 (Cap Bottom Plate)	µm
Poly 2 (width/space)	0.8/1.0 (CMOS Gate and Cap Top Plate)	µm
Contact (width/space)	0.8/0.8	µm
Via 1 (width/space)	0.8/1.0	µm
Via 2 (width/space)	0.8/1.0	µm
Metal 1 (width/space)	1.4/1.0	µm
Metal 2 (width/space)	1.4/1.0	µm
Metal 3 (width/space)	1.4/1.2	µm

Typical Electrical Parameters (175 Å Gate Oxide)

	N-CH	P-CH	Units
Vt(30X0.8 µm)	0.87	-0.91	V
Ids	0.32	-0.18	mA/µm
Gain µC (30X30)	91	31	$\mu A/V^2$
Body Effect	0.5	0.35	$V^{1/2}$
Sub-threshold slope	90	90	mV/decade
Leff	0.6	0.7	µm
Xj	0.28	0.28	µm
Rs	46	92	Ω/square
Rs poly	— 31	—	Ω/square

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