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0.6μm CMOS Process

Standard Features

- Single or double poly
- Double metal
- 5.5V max operating voltage
- Twin well

Process Technology

- 5X Stepper
- EPI starting material provides latch-up protection
- Double well implant
- Ldd for hot electron reliability
- Sandwich metal for e-m
- Titanium nitride barrier metal

Standard Layout Rules and Process Parameters

	Values	Units
Min gate length (N&P)	0.6	μm
Gate oxide	130	Å
Inter-poly dielectric (oxide equiv.)	525	Å
Active (width/space)	0.6/1.0	μm
Poly 1 (width/space)	0.6/0.7 (Cap Bottom Plate)	μm
Poly 2 (width/space)	0.6/0.7 (CMOS Gate and Cap Top Plate)	μm
Contact (width/space)	0.6/0.6	μm
Via (width/space)	0.6/0.8	μm
Metal 1 (width/space)	0.8/0.8	μm
Metal 2 (width/space)	0.8/0.9	μm

Typical Electrical Parameters

	N-CH	P-CH	Units
Vt(30X0.8 μm)	0.92	-0.85	V
Ids	0.51	-0.27	mA/μm
Gain μC (30X30)	110	38	μA/V^2
Body Effect	0.45	0.32	$V^{1/2}$
Sub-threshold slope	90	90	mV/decade
Leff	0.48	0.6	μm
Xj	0.27	0.21	μm
Rs	39	100	Ω/square
Rs poly	— 24	—	Ω/square

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