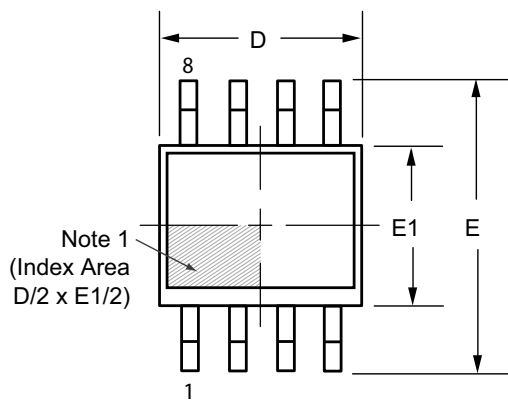
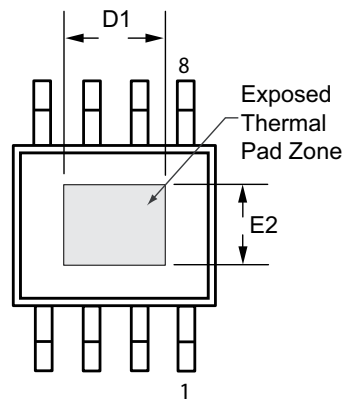


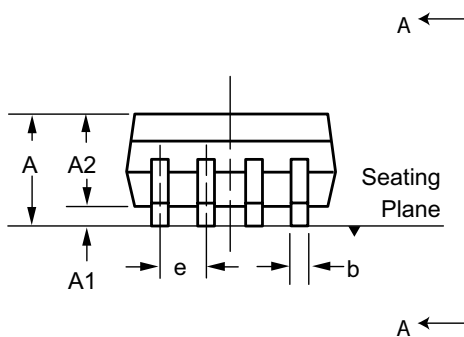
8-Lead SOIC (Narrow Body w/Heat Slug) Package Outline (SG)
4.90x3.90mm body, 1.70mm height (max), 1.27mm pitch



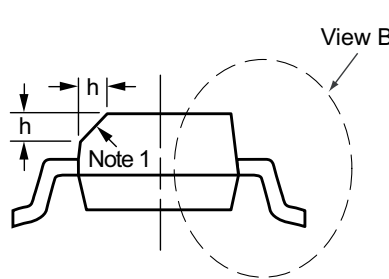
Top View



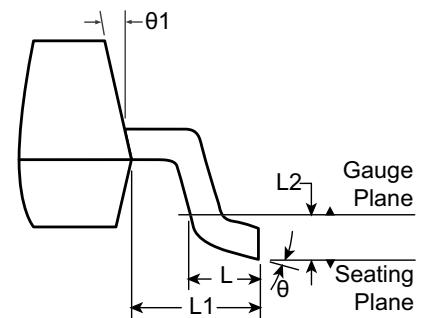
Bottom View



Side View



View A - A



View B

Note:
 1. If optional chamfer feature is not present, a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	E2	e	h	L	L1	L2	θ	θ1			
Dimension (mm)	MIN	1.25*	0.00	1.25	0.31	4.80*	3.30†	5.80*	3.80*	2.29†	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°		
	NOM	-	-	-	-	4.90	-	6.00	3.90	-		-	-			-	-	-	-
	MAX	1.70	0.15	1.55*	0.51	5.00*	3.81†	6.20*	4.00*	2.79†		0.50	1.27			8°	15°		

JEDEC Registration MS-012, Variation BA, Issue E, Sept. 2005.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-8SOSG, Version D041009.

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