MD1711 + TC6320 Demoboard
Five-Level, Dual Channel ±100V 2.0A RTZ Pulser

Features

- Five-level, dual-channel ultrasound transmitter
- MD1711 driving six TC6320 HV MOSFETs
- Design for RTZ waveforms outputs
- Low second harmonic distortion
- Dual 0 to +/-100V peak to peak voltage supply
- ±2.0 A source and sink current capability
- SMA connectors for external clock and signals
- 1.8 to 3.3V CMOS logic interface

Applications

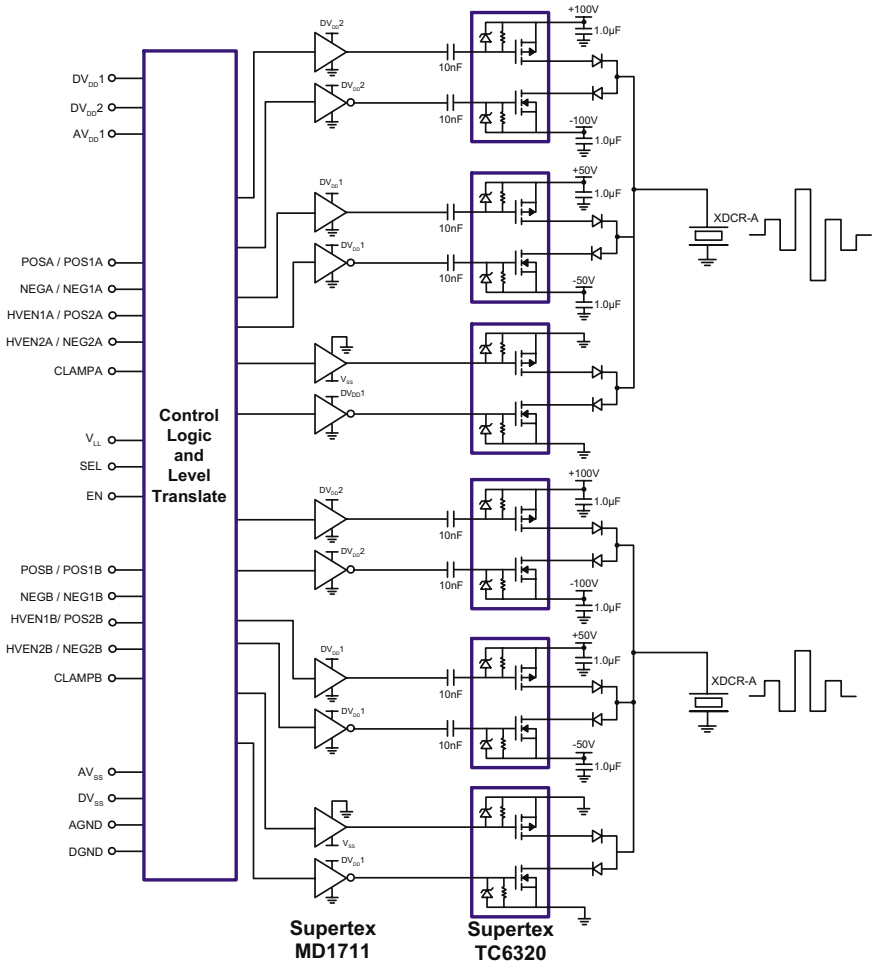
- Medical ultrasound imaging
- Ultrasonic NDT inspection
- Piezoelectric transducer drivers
- ATE and waveform generator
- PZT transducer drivers
- Capacitive and MEMS sensor driver

General Description

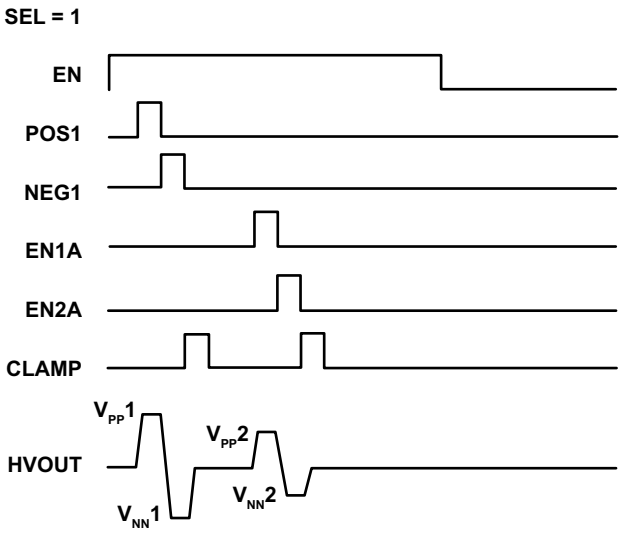
The MD1711DB2 demoboard is as a five-level, dual-channel, +/-100V, 2.0A, return-to-zero pulser. It can directly drive two 50 or 75Ω impedance transducers for 1.0MHz to 20MHz medical ultrasound imaging or NDT applications.

The MD1711DB2 consists of one MD1711 in a 48-Lead LQFP package driving six TC6320 complementary high voltage MOSFET pairs in 8-Lead SOIC packages. The external logic signal connector, J13, connects all the input control signals of the MD1711 to the user's logic control source via a short ribbon cable. In typical two-, three- or five-level bipolar pulsing, PW or CW waveforms can be generated by the proper input control signal listed below. Jumpers are provided for the output, such that it can drive either the on-board RC load 220pF capacitor in parallel with a 1.0KΩ resistor or with an external load of cable to the user's ultrasound testing transducer.

Block Diagram

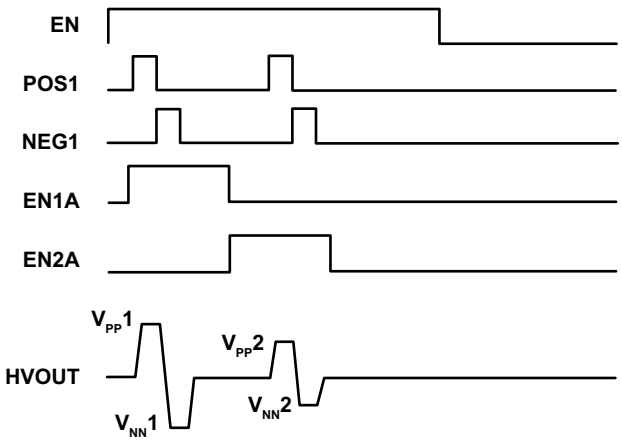


Demo Waveform A

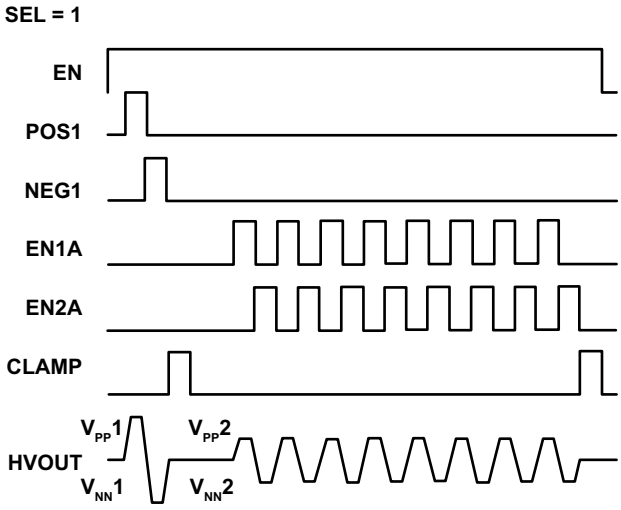


Demo Waveform B

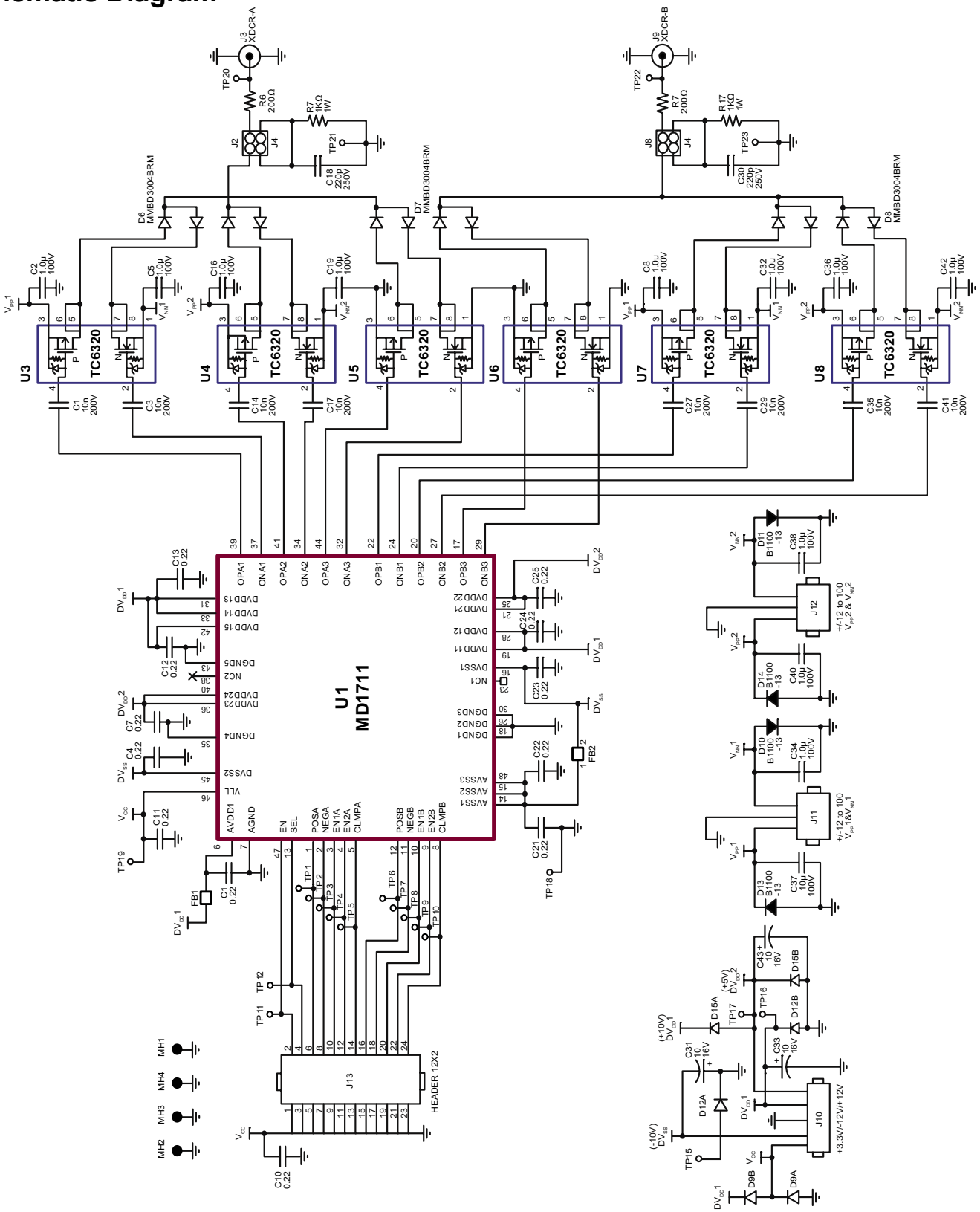
SEL = 0, CLAMP = 0



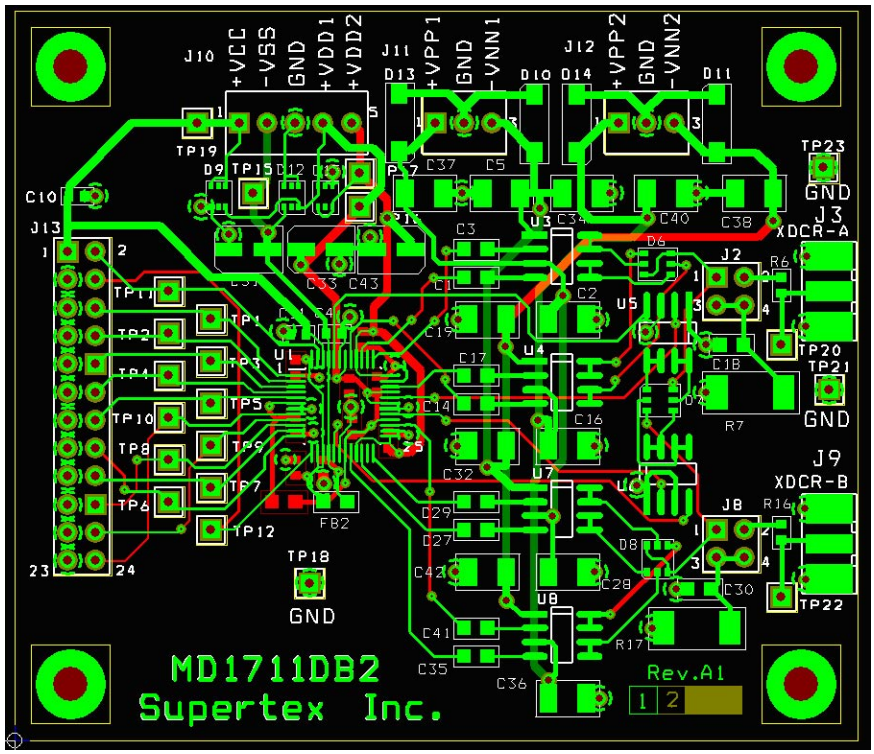
Demo Waveform C



Schematic Diagram



PCB Layout



Power Supply Voltages and Current Limit Settings

Sym	Parameter	Min	Typ	Max	Units	Suggested Current Limit
VSS	Negative drive supply	-12	-10	-8.0	V	10mA
VDD1	Positive drive supply	8.0	10	12.6	V	50mA
VDD2	Positive drive supply	4.75	5.0	12.6	V	10mA
VCC	Logic Supply MD1711 VLL	1.8	3.3	5.5	V	5.0mA (not including to J13-1, if any)
VPP1	TC6320 HV positive supply	0	-	100	V	1.5mA
VNN1	TC6320 HV negative supply	-100	-	0	V	1.5mA
VPP2	TC6320 HV positive supply	0	-	100	V	1.5mA
VNN2	TC6320 HV negative supply	-100	-	0	V	1.5mA

Voltage Supply Power-Up Sequence

1	VCC	+1.8V to +3.3V positive logic voltage for VCC and VLL
2	VDD1	+10V positive drive voltage for DVDD1
3	VDD2	+5.0V positive drive voltage for DVDD2
4	VSS	-10V negative bias voltage for DVSS and AVSS
5	VPP1/VNN1	0 to +/-100V 1st positive and negative high voltage
6	VPP2/VNN2	0 to +/-100V 2nd positive and negative high voltage

Testing MD1711DB2 Ultrasound Pulser

Power supply voltages and current limit settings to start the power-up sequence are listed above. Power-down is the reverse of the power-up sequence.

It is important to have the protective Schottky diodes on the MD1711 and the TC6320 pulser circuit PCB on each voltage-rail, just like this demoboard. Only one set of diodes is required per board if multiple pulser channels are on the same PCB. The IC substrate of the MD1711 is internally connected to the AVSS pin. While powering up a multi-voltage rail CMOS chip, one must usually turn one of the substrate bias voltages first, in order to prevent CMOS latch-up. However, with the Schottky diodes on-board, specifically the D9, D12 and D15 diodes, the MD1711 is allowed to power-on the VCC +3.3V first, to establish the CPU and FPGA, etc. and get the digital circuit working first, then power-on the AVSS/DVSS, AVDD/DVDD and VPP/VNN, etc., with the inactive input logic known-state.

Use a ribbon cable to connect the input logic signal connector, J13. Ground pins 3, 5-23 of J13 on the digital logic DGND of the signal generator side. Logic supply voltage V_{CC} must equal the V_{LL} of MD1711. It is usually 1.8, 2.5 or 3.3V DC.

Use a high-impendence oscilloscope probe for all on-board test points. There are two 5:1 voltage attenuators on-board (R6 and R16 are 200Ω) that are designed to connect the high voltage output J3 and J9 SMA connectors via a 50Ω coaxial cable to the oscilloscope (50Ω input) directly. If one needs to connect the J3 or J9 SMA connectors to a testing transducer with a coaxial cable of 50/75Ω, in order to prevent circuit damage due to long cable line reflection, a proper in-series resistor of 40 to 67Ω revise-termination should be considered on R6 or R16, with the impedance matching the cable and transducer load impedances. The TC6320's output impedance is about 8.0Ω.

If an external cable load is used, disconnect the on-board load (220pF // 1.0KΩ) by removing both jumpers on J2 or J8 (1-3) & (2-4), then place one jumper at J2 or J8 (1-2) position. Any overloaded outputs, including shorter pulse duty cycles, longer pulse durations or higher CW voltages (>12V) could damage the IC or MOSFETs.

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