

40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- ▶ HVCMOS® technology
- ▶ 5.0V logic and 12V supply rail
- ▶ Output voltage up to +200V
- ▶ Low power level shifting
- ▶ Source/sink current minimum 50mA
- ▶ 40MHz equivalent data rate
- ▶ Latched data outputs
- ▶ Forward and reverse shifting options (DIR pin)
- ▶ Chip select
- ▶ Polarity function

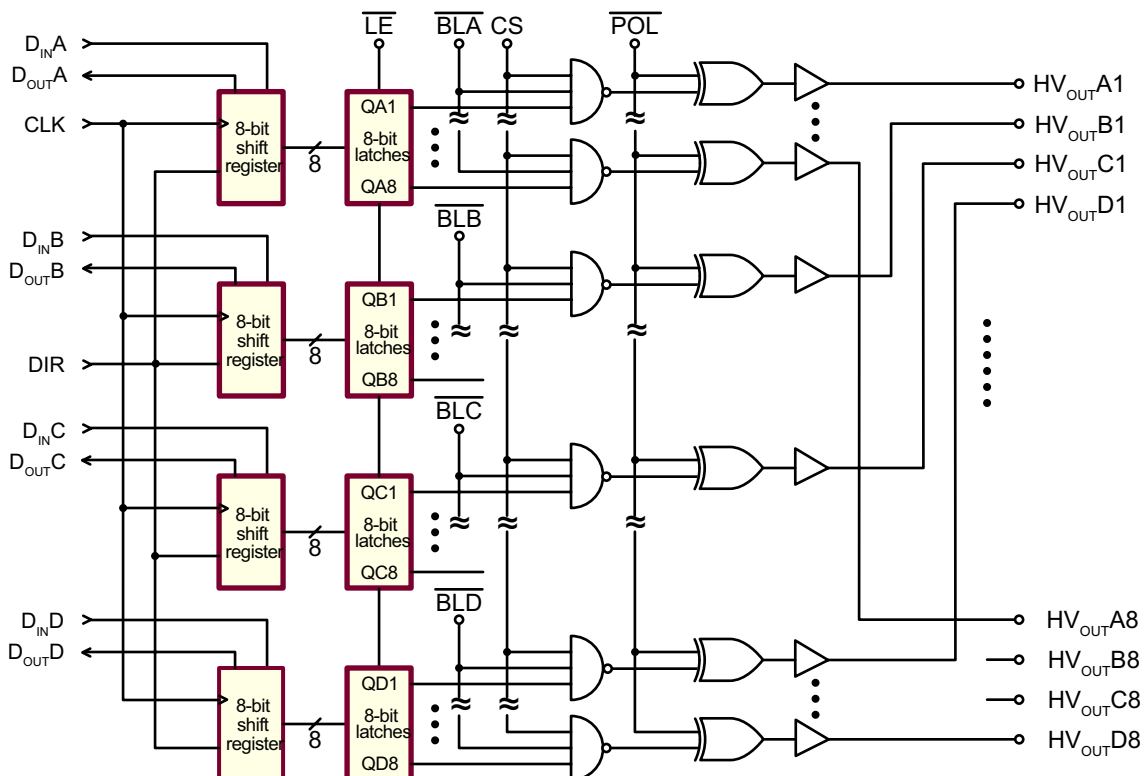
General Description

The HV7620 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rates four times the speed of one. The data is clocked in simultaneously on all four data inputs with a single clock. Data is shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to VDD1, and counterclockwise (CCW) shifting when connected to GND. Operation of the shift register is not affected by the \overline{LE} (latch enable) input. Transfer of data from the shift registers to the latches occurs when the \overline{LE} input is high. Data is stored in the latches when \overline{LE} is low. The current source on the logic inputs provides active pull up when the input pins are open.

Functional Block Diagram



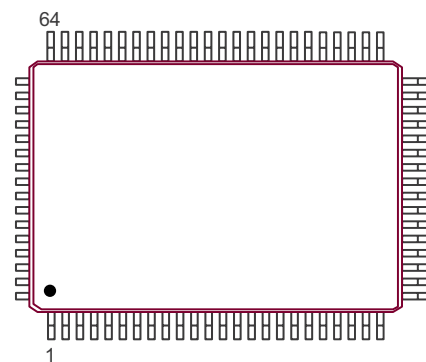
Ordering Information

Device	64-Lead PQFP 20.00x14.00mm body 3.40mm height (max) 0.80mm pitch 3.90mm footprint
HV7620	HV7620PG-G

-G indicates package is RoHS compliant ("Green")



Pin Configuration



64-Lead PQFP (PG)
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD1}	-0.5V to +15V
Supply voltage, V_{DD2}	-0.5V to +15V
Supply voltage, V_{PP}	-0.5V to +225V
Logic input levels	-2.0V to $V_{DD1} + 2.0V$
Continuous total power dissipation ¹	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Notes:

- For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.

Recommended Operating Conditions

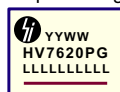
Sym	Parameter	Min	Max	Units	
V_{DD1}	Logic supply voltage	4.5	V_{DD2}	V	
V_{DD2}	12V supply voltage	10.8	13.2	V	
V_{PP}	High voltage supply voltage	50	200	V	
V_{IH}	High-level input voltage	$V_{DD1} - 0.5V$	V_{DD1}	V	
V_{IL}	Low-level input voltage	0	0.5	V	
f_{CLK}	Clock frequency	$V_{DD1} = 5.0V$	-	10	MHz
		$V_{DD1} = 12V$	-	5	MHz
T_A	Operating temperature range	-40	+85	°C	
I_{OD}	Allowable pulsed current through output diodes ¹	-	500	mA	
$I_{GND(VPP)}$	Allowable pulsed V_{PP} or HVGND current ¹	-	16	A	
$V_{PP(SLEW)}$	Slew rate of V_{PP}	-	340	V/μs	

Notes:

- The current pulse width = 500ns, duty cycle = 5%.

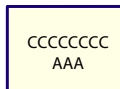
Product Marking

Top Marking



YY = Year Sealed
 WW = Week Sealed
 L = Lot Number
 C = Country of Origin*
 A = Assembler ID*

Bottom Marking



— = "Green" Packaging
 *May be part of top marking

Package may or may not include the following marks: Si or

64-Lead PQFP (PG)

DC Electrical Characteristics

(Over operating supply voltages and temperature, unless otherwise noted, $V_{DD1} = 5.0V$, $V_{DD2} = 12V$, $V_{PP} = 200V$ and $T_A = 25^\circ C$)

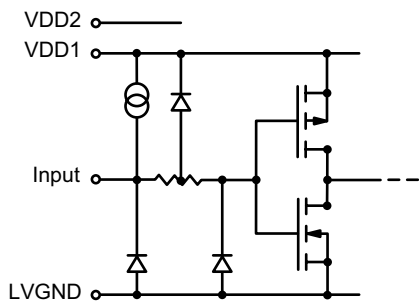
Sym	Parameter	Min	Max	Units	Conditions
I_{DD1}	V_{DD1} supply current	-	5.0	mA	$f_{CLK} = 10MHz$
I_{DD2}	V_{DD2} supply current	-	20	mA	$V_{DD2} = V_{DD2} \text{ max}$, $f_{CLK} = 10MHz$
I_{PP}	High voltage supply current	-	2.0	mA	All outputs high or low
I_{DD1Q}	Quiescent V_{DD1} supply current	-	100	μA	All input = V_{DD1}
I_{DD2Q}	Quiescent V_{DD2} supply current	-	100	μA	All input = V_{DD1}
V_{OH}	High-level output	185	-	V	$I_O = -50mA$
V_{OL}	Low-level output	-	20	V	$I_O = +50mA$
I_{IH}	High-level logic input current	-	1.0	μA	$V_{IN} = V_{DD1}$
I_{IL}	Low-level logic input current	-	-10	μA	$V_{IN} = 0V$
V_{GG}	HVGND to LVGND voltage difference	-1.0	1.0	V	---

AC Electrical Characteristics

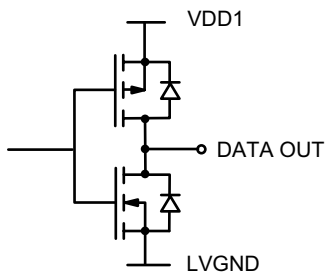
(Logic signal inputs and data inputs have $t_r, t_f \leq 5ns$. $V_{DD1} = 5.0V$ or $12V$, $V_{DD2} = 12V$, $V_{PP} = 200V$)

Sym	Parameter	Min	Max	Units	Conditions	
f_{CLK}	Clock frequency	$V_{DD1} = 5.0V$	-	10	MHz	Per register, $C_L = 15pF$
		$V_{DD1} = 12V$	-	5.0		
t_{WL}, t_{WH}	Clock width high or low	40	-	ns	---	
t_{SU}	Data set-up time before clock rises	20	-	ns	---	
t_H	Data hold time after clock rises	20	-	ns	---	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	-	275	ns	$C_L = 15pF$	
t_{WLE}	\overline{LE} pulse width	25	-	ns	---	
t_{DLE}	Delay time clock to \overline{LE} low to high	50	-	ns	---	
t_{SLE}	\overline{LE} set-up time before clock rises	20	-	ns	---	
t_{DLF}, t_{DLN}	\overline{BL} or CS low to high to HV_{OUT}	-	250	ns	---	
t_{COF}, t_{CON}	Clock to HV_{OUT}	-	275	ns	---	
t_{DLH}	Delay time clock to data low to high	-	100	ns	$C_L = 15pF$	
t_{DHL}	Delay time clock to data high to low	-	100	ns	$C_L = 15pF$	

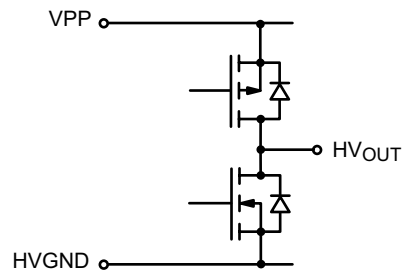
Input and Output Equivalent Circuits



Logic Inputs

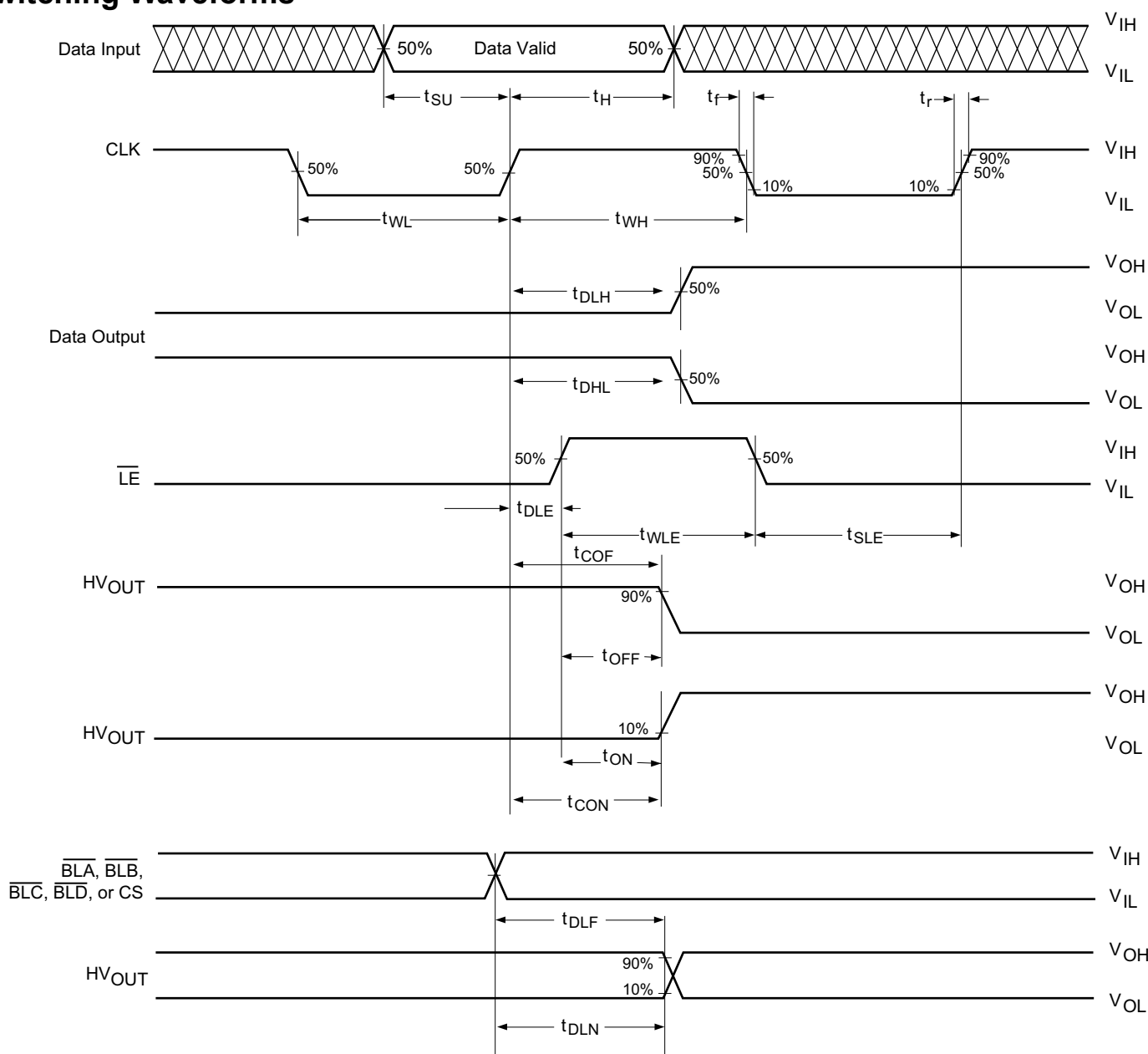


Logic Data Output



High Voltage Outputs

Switching Waveforms



Function Table

Function	Inputs													Outputs			
	D _{IN} A	D _{IN} B	D _{IN} C	D _{IN} D	CLK	\overline{LE}	DIR	\overline{BLA}	\overline{BLB}	\overline{BLC}	\overline{BLD}	CS	\overline{POL}	A	B	C	D
All O/P High	X	X	X	X	X	X	X	X	X	X	X	L	L	H	H	H	H
All O/P Low	X	X	X	X	X	X	X	X	X	X	X	L	H	L	L	L	L
“A” Outputs Low	X	X	X	X	X	X	X	L	X	X	X	X	H	L	*	*	*
Normal Polarity	X	X	X	X	X	X	X	H	H	H	H	H	H	No Inversion			
Outputs Inverted	X	X	X	X	X	X	X	H	H	H	H	H	L	Inversion			
Transparent Mode	H	L	L	L	↑	H	X	H	H	H	H	H	H	H	L	L	L
Data Stored	X	X	X	X	X	L	X	H	H	H	H	H	H	Stored data			
Shift CW	X	X	X	X	↑	H	H	H	H	H	H	H	X	A _N → A _{N+1}	B _N → B _{N+1}	C _N → C _{N+1}	D _N → D _{N+1}
Shift CCW	X	X	X	X	↑	H	L	H	H	H	H	H	X	A _N → A _{N-1}	B _N → B _{N-1}	C _N → C _{N-1}	D _N → D _{N-1}

Notes:

H = High level, L = Low level, X = Irrelevant, ↑ = Low to high transition.

* = Dependent on previous stage's state before the last CLK ↑ for last \overline{LE} high.

Power-up sequence:

1. GND (HV, LV)
2. V_{DD1}
3. V_{DD2}
4. V_{PP}
5. Logic Input Signals

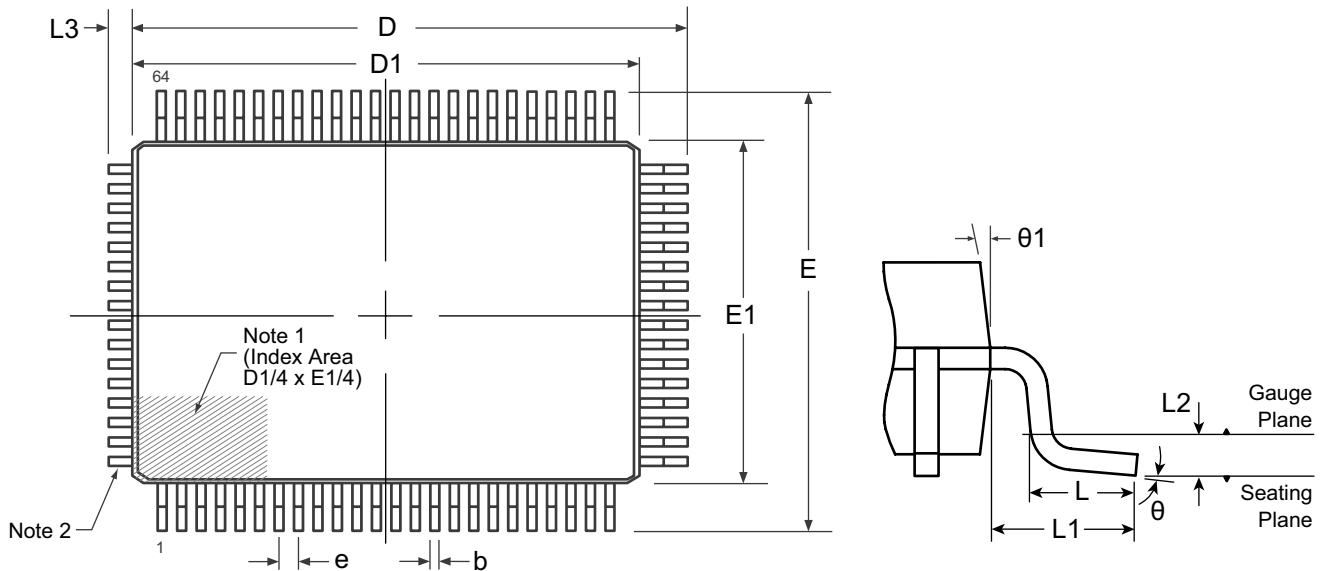
To power down reverse the sequence above.

Pin Function

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	HVGND	17	HV _{OUT} B5	33	CS	49	HV _{OUT} B4
2	VPP	18	HV _{OUT} A5	34	D _{OUT} B	50	HV _{OUT} A4
3	HV _{OUT} D8	19	VPP	35	D _{IN} B	51	HV _{OUT} D3
4	HV _{OUT} C8	20	HVGND	36	D _{IN} A	52	HV _{OUT} C3
5	HV _{OUT} B8	21	HVGND	37	D _{OUT} A	53	HV _{OUT} B3
6	HV _{OUT} A8	22	VDD2	38	CLK	54	HV _{OUT} A3
7	HV _{OUT} D7	23	$\overline{\text{BLC}}$	39	$\overline{\text{BLA}}$	55	HV _{OUT} D2
8	HV _{OUT} C7	24	$\overline{\text{BLD}}$	40	$\overline{\text{BLB}}$	56	HV _{OUT} C2
9	HV _{OUT} B7	25	$\overline{\text{LE}}$	41	VDD1	57	HV _{OUT} B2
10	HV _{OUT} A7	26	D _{OUT} D	42	LVGND	58	HV _{OUT} A2
11	HV _{OUT} D6	27	D _{IN} D	43	N/C	59	HV _{OUT} D1
12	HV _{OUT} C6	28	D _{IN} C	44	HVGND	60	HV _{OUT} C1
13	HV _{OUT} B6	29	D _{OUT} C	45	HVGND	61	HV _{OUT} B1
14	HV _{OUT} A6	30	$\overline{\text{POL}}$	46	VPP	62	HV _{OUT} A1
15	HV _{OUT} D5	31	LVGND	47	HV _{OUT} D4	63	VPP
16	HV _{OUT} C5	32	DIR	48	HV _{OUT} C4	64	HVGND

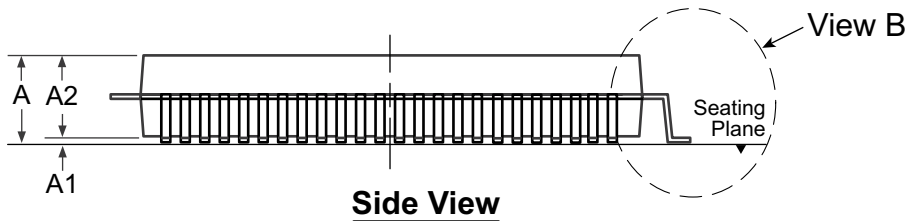
64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View

View B



Side View

- Note:**
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 Identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
 2. The leads on this side are trimmed.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1	
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.
Supertex Doc. #: DSPD-64PQFP, Version NR090608.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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