

64-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

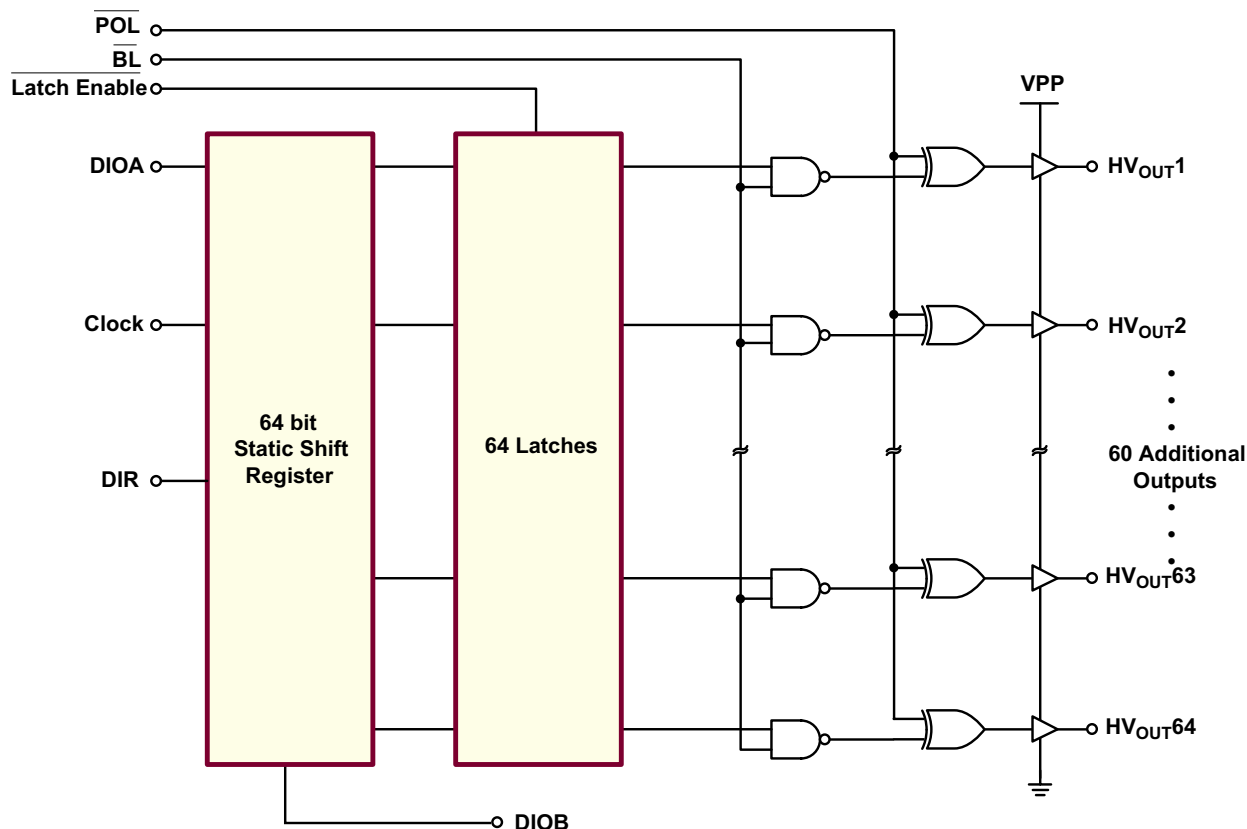
- ▶ Processed with HVCMOS® technology
- ▶ Output voltages to 180V
- ▶ Low power level shifting
- ▶ Shift register speed:
 - 6.0MHz @ $V_{DD} = 5.0V$
 - 12MHz @ $V_{DD} = 12V$
- ▶ Latched data outputs
- ▶ Output polarity and blanking
- ▶ CMOS compatible inputs
- ▶ Forward and reverse shifting options

General Description

The HV3418 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for inkjet applications. It can also be used in any application requiring multiple output, high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, D_{IOA} is Data-In and D_{IOB} is Data-Out; data is shifted from HV_{OUT64} to HV_{OUT1} . When DIR is at logic high, D_{IOB} is Data-In and D_{IOA} is Data-Out; data is then shifted from HV_{OUT1} to HV_{OUT64} . Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the \overline{LE} (latch enable), \overline{BL} (blanking), or the \overline{POL} (polarity) inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} (latch enable) is high. The data in the latch is stored during \overline{LE} transition from high to low.

Functional Block Diagram



Ordering Information

Device	Package Options	
	80-Lead CQFP Ceramic 20.00x14.00mm body 3.40mm height (max) 0.80mm pitch	80-Lead PQFP 20.00x14.00mm body 3.40mm height (max) 0.80mm pitch
HV3418	HV3418DG	HV3418PG-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.5V to +15V
Output voltage, V_{PP}	V_{DD} to +200V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current ¹	1.5A
High voltage supply current ¹	1.3A
Continuous total power dissipation ²	Plastic: 1200mW Ceramic: 1900mW
Operating temperature range	Ceramic: -55°C to +125°C Plastic: -40°C to +85°C
Storage temperature range	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

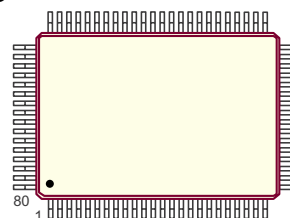
Notes:

1. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic, and at 31.7mW/°C for ceramic.

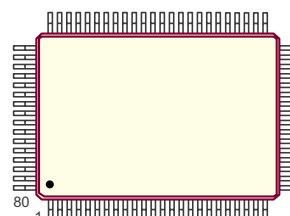
Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	
V_{DD}	Logic supply voltage	$V_{DD} = 5.0V$	4.5	5.0	5.5	V
		$V_{DD} = 12V$	10.8		13.2	
V_{PP}	High voltage supply	60	-	180	V	
V_{IH}	High-level input voltage	$V_{DD} - 0.9$	-	V_{DD}	V	
V_{IL}	Low-level input voltage	0	-	0.9	V	
T_A	Operating free-air temperature					°C
	Ceramic:	-55		+125		
	Plastic:	-40		+85		

Pin Configurations



80-Lead CQFP Ceramic (DG)
(top view)



80-Lead PQFP (PG)
(top view)

Product Markings

HV3418DG LLLLLLLLLL YYWW CCCCCC AAA	L = Lot Number YY = Year Sealed WW = Week Sealed C = Country of Origin A = Assembler ID
--	---

80-Lead CQFP Cerpak (DG)

HV3418PG LLLLLLLLLL YYWW CCCCCC AAA	L = Lot Number YY = Year Sealed WW = Week Sealed C = Country of Origin A = Assembler ID ___ = "Green" Packaging
--	--

80-Lead PQFP (PG)

Power-up sequence should be the following:

1. Connect ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, Enable, etc.) to a known state
4. Apply V_{PP}

The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics (Over recommended operating conditions unless otherwise noted)

Sym	Parameter	Min	Max	Units	Conditions	
I_{DD}	V_{DD} supply current	-	25	mA	$f_{CLK} = 12\text{MHz}$, $f_{DATA} = 12\text{MHz}$, $\overline{LE} = \text{low}$	
I_{DDQ}	Quiescent V_{DD} supply current	-	200	μA	All $V_{IN} = 0$ or V_{DD}	
I_{PP}	High voltage supply current	-	0.50	mA	$V_{PP} = 180\text{V}$. All outputs high.	
		-	0.50		$V_{PP} = 180\text{V}$. All outputs low.	
I_{IH}	High-level logic input current	-	10	μA	$V_{IH} = V_{DD}$	
I_{IL}	Low-level logic input current	-	-10	μA	$V_{IL} = 0\text{V}$	
V_{OH}	High level output	HV_{OUT}	155	-	V	$V_{PP} = 180\text{V}$, $I_{HV_{OUT}} = -5.0\text{mA}$, $I_{D_{OUT}} = -100\mu\text{A}$
		D_{OUT}	$V_{DD} - 1.0\text{V}$	-		
V_{OL}	Low level output	HV_{OUT}	-	25	V	$V_{PP} = 180\text{V}$, $I_{HV_{OUT}} = +5.0\text{mA}$, $I_{D_{OUT}} = +100\mu\text{A}$
		D_{OUT}	-	1.0		
V_{OC}	HV_{OUT} clamp voltage	-	$V_{DD} + 1.5\text{V}$	V	$I_{OL} = +5.0\text{mA}$	
		-	-1.5		$I_{OL} = -5.0\text{mA}$	

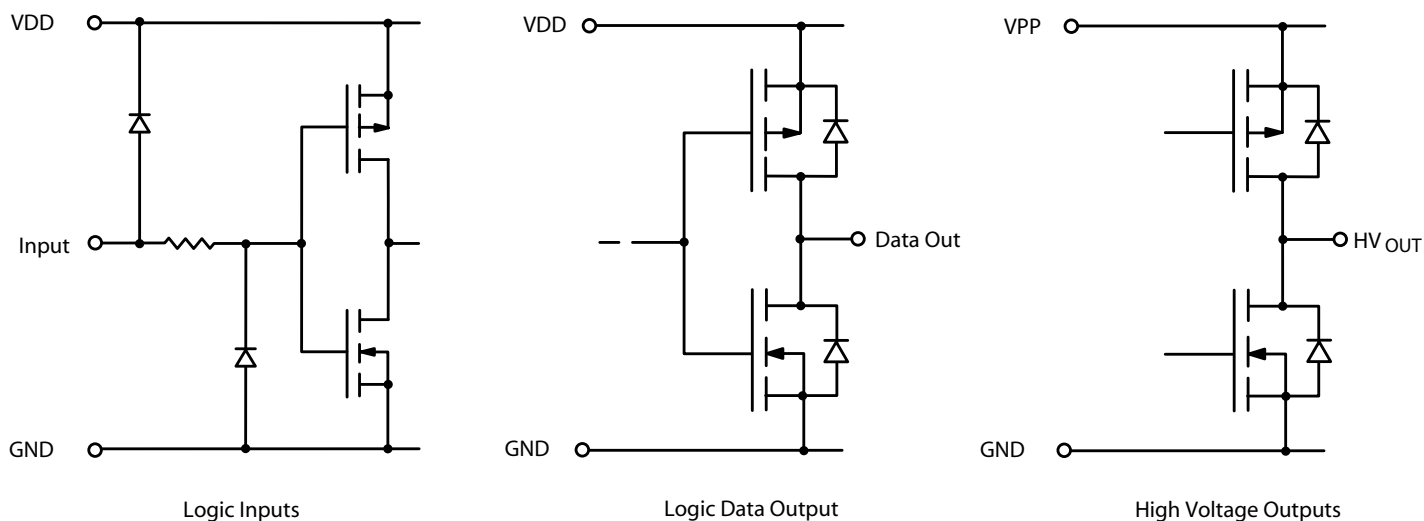
AC Electrical Characteristics (For $V_{DD} = 12\text{V}$. Values in parantheses are for $V_{DD} = 5.0\text{V}$, $V_{PP} = 180\text{V}$, $T_A = 25^\circ\text{C}$)

Sym	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	-	12 (6.0)	MHz	---
t_W	Clock width high or low	40 (83)	-	ns	---
t_{SU}	Data set-up time before clock rises	25 (35)	-	ns	---
t_H	Data hold time after clock rises	10 (30)	-	ns	---
t_{WLE}	\overline{LE} pulse width	62 (80)	-	ns	---
t_{DLE}	Delay time clock to \overline{LE} high to low	25 (35)	-	ns	---
t_{SLE}	\overline{LE} set-up time before clock rises	30 (40)	-	ns	---
t_{ON} , t_{OFF}	Time from \overline{LE} to HV_{OUT}	-	1.0 (1.5)	μs	$C_L = 20\text{pF}$
t_{DHL}	Delay time clock to data high to low	-	50 (110)	ns	$C_L = 20\text{pF}$
t_{DLH}	Delay time clock to data low to high	-	75 (160)	ns	$C_L = 20\text{pF}$
t_r , t_f	All logic inputs	-	5.0	ns	---

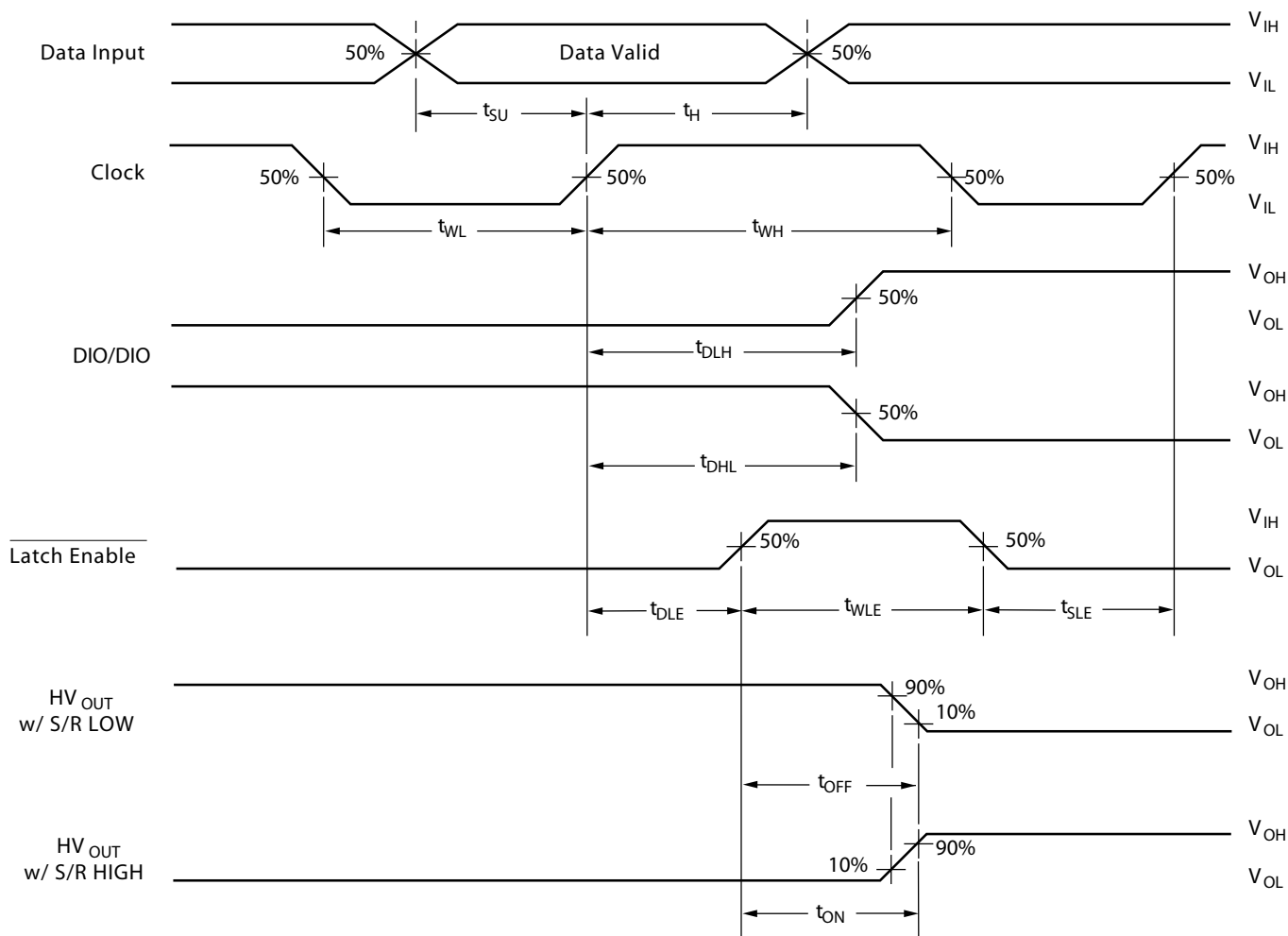
Notes:

- Shift register speed can be as low as DC as long as data set-up and hold time meet the spec.
- AC characteristics are guaranteed only under $V_{DD} = 12\text{V}$ and $V_{DD} = 5.0\text{V}$.

Input and Output Equivalent Circuits



Switching Waveforms



Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{\text{LE}}$	$\overline{\text{BL}}$	$\overline{\text{POL}}$	DIR	Shift Reg		HV Outputs		Data Out
							1	2...64	1	2...64	*
All on	X	X	X	L	L	X	*	*...*	H	H...H	*
All off	X	X	X	L	H	X	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*...*	*	*...*	*
Load/store data in latches	X	X	↓	H	H	X	*	*...*	*	*...*	*
	X	X	↓	H	L	X	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	X	L	*...*	L	*...*	*
	H	↑	H	H	H	X	H	*...*	H	*...*	*
I/O relation	DIOA	↑	X	X	X	L	$Q_N \rightarrow$	Q_{N+1}	-	-	DIOB
	DIOB	↑	X	X	X	H	$Q_N \rightarrow$	Q_{N+1}	-	-	DIOA

Notes:

H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.

* = dependent on previous stage's state before the last CLK or last $\overline{\text{LE}}$ high.

Pin Description (DG, PG)

Pin #	Function
1	HV _{OUT} 41/24
2	HV _{OUT} 42/23
3	HV _{OUT} 43/22
4	HV _{OUT} 44/21
5	HV _{OUT} 45/20
6	HV _{OUT} 46/19
7	HV _{OUT} 47/18
8	HV _{OUT} 48/17
9	HV _{OUT} 49/16
10	HV _{OUT} 50/15
11	HV _{OUT} 51/14
12	HV _{OUT} 52/13
13	HV _{OUT} 53/12
14	HV _{OUT} 54/11
15	HV _{OUT} 55/10
16	HV _{OUT} 56/9
17	HV _{OUT} 57/8
18	HV _{OUT} 58/7
19	HV _{OUT} 59/6
20	HV _{OUT} 60/5
21	HV _{OUT} 61/4
22	HV _{OUT} 62/3
23	HV _{OUT} 63/2
24	HV _{OUT} 64/1
25	VPP
26	DIOA
27	N/C
28	N/C
29	$\overline{\text{BL}}$
30	$\overline{\text{POL}}$
31	VDD
32	DIR
33	LGND
34	OGND
35	N/C
36	N/C
37	CLK
37	$\overline{\text{LE}}$
39	DIOB
40	VPP

Pin #	Function
41	HV _{OUT} 1/64
42	HV _{OUT} 2/63
43	HV _{OUT} 3/62
44	HV _{OUT} 4/61
45	HV _{OUT} 5/60
46	HV _{OUT} 6/59
47	HV _{OUT} 7/58
48	HV _{OUT} 8/57
49	HV _{OUT} 9/56
50	HV _{OUT} 10/55
51	HV _{OUT} 11/54
52	HV _{OUT} 12/53
53	HV _{OUT} 13/52
54	HV _{OUT} 14/51
55	HV _{OUT} 15/50
56	HV _{OUT} 16/49
57	HV _{OUT} 17/48
58	HV _{OUT} 18/47
59	HV _{OUT} 19/46
60	HV _{OUT} 20/45
61	HV _{OUT} 21/44
62	HV _{OUT} 22/43
63	HV _{OUT} 23/42
64	HV _{OUT} 24/41
65	HV _{OUT} 25/40
66	HV _{OUT} 26/39
67	HV _{OUT} 27/38
68	HV _{OUT} 28/37
69	HV _{OUT} 29/36
70	HV _{OUT} 30/35
71	HV _{OUT} 31/34
72	HV _{OUT} 32/33
73	HV _{OUT} 33/32
74	HV _{OUT} 34/31
75	HV _{OUT} 35/30
76	HV _{OUT} 36/29
77	HV _{OUT} 37/28
78	HV _{OUT} 38/27
79	HV _{OUT} 39/26
80	HV _{OUT} 40/25

Notes:

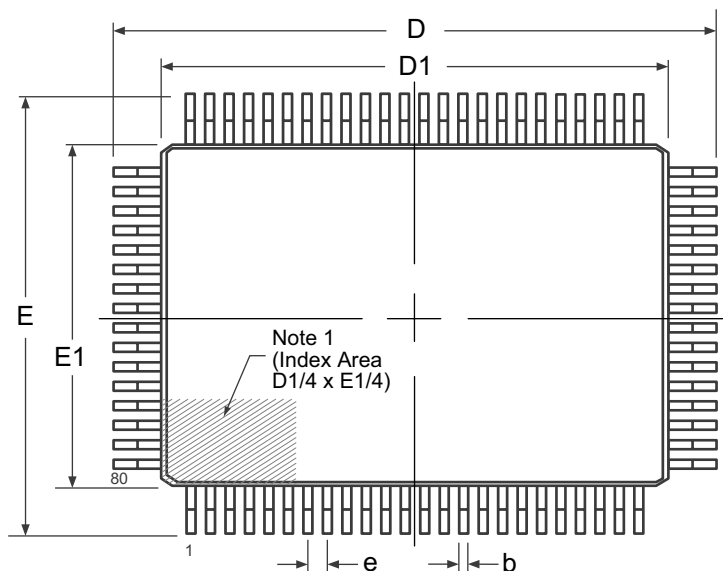
Pin designation for DIR = H/L

Example:

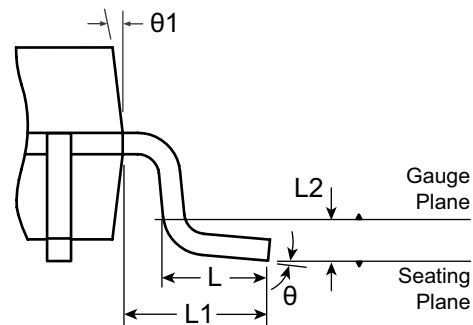
for DIR = H, Pin 1 is HV_{OUT}41for DIR = L, Pin 1 is HV_{OUT}24

80-Lead CQFP (Ceramic) Package Outline (DG)

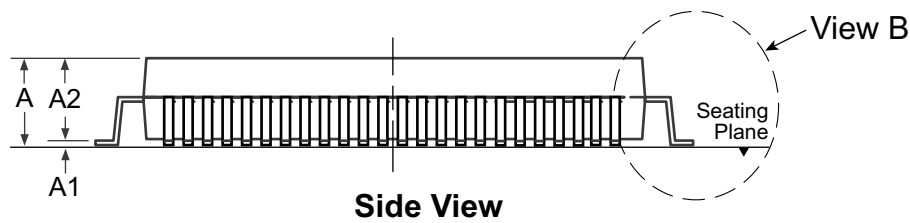
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue A, Sept 1995.

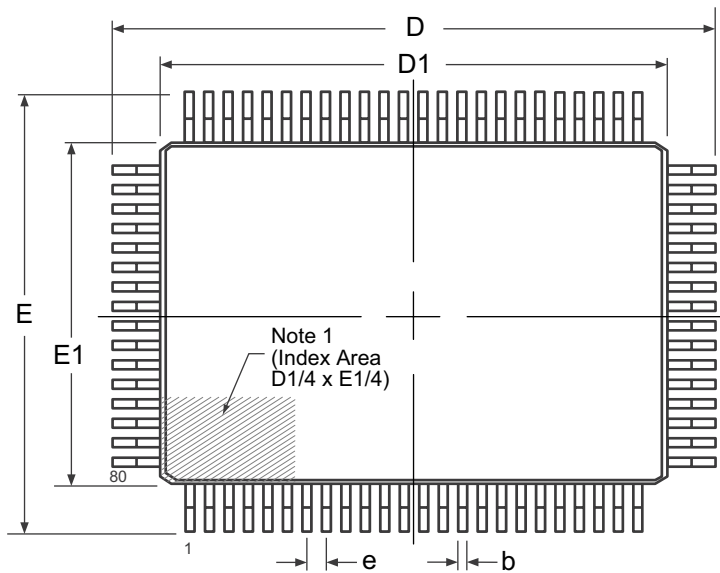
* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

Drawings not to scale.

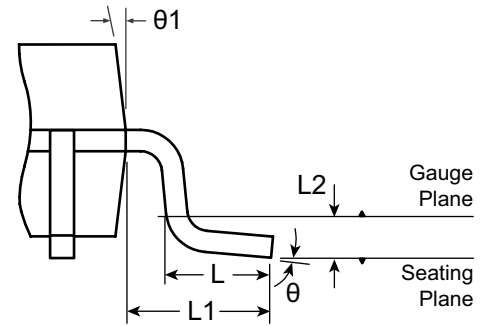
Supertex Doc. #: DSPD-80CQFPDG, Version NR103008.

80-Lead PQFP Package Outline (PG)

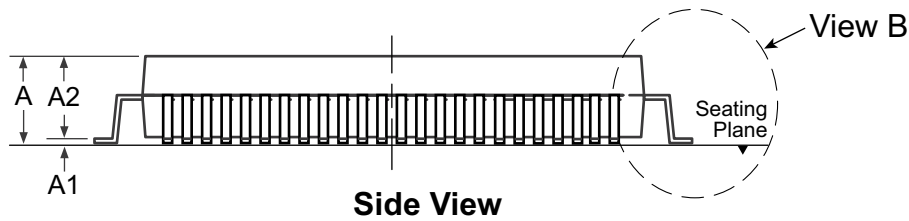
20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Top View



View B



Side View

Note:
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1	
Dimension (mm)	MIN	2.80*	0.25	2.55	0.30	23.65*	19.80*	17.65*	13.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°	5°
	NOM	-	-	2.80	-	23.90	20.00	17.90	14.00		0.88			3.5°	-
	MAX	3.40	0.50*	3.05	0.45	24.15*	20.20*	18.15*	14.20*		1.03			7°	16°

JEDEC Registration MO-112, Variation CB-1, Issue B, Sept. 1995.
 * This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.
Drawings not to scale.
Supertex Doc. #: DSPD-80PQFPPG, Version B101708.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." Supertex inc. does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the Supertex inc. website: <http://www.supertex.com>.