

# Low Charge Injection 32-Channel High Voltage Analog Switch with Bleed Resistors

## Features

- ▶ 32 Channels of high voltage analog switch
- ▶ Integrated bleed resistors on the outputs
- ▶ 2:1 Multiplexer / Demultiplexer
- ▶ 3.3V or 5.0V CMOS input logic level
- ▶ 30MHz data shift clock frequency
- ▶ HVCMOS technology for high performance
- ▶ Very low quiescent power dissipation -10µA
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

## Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

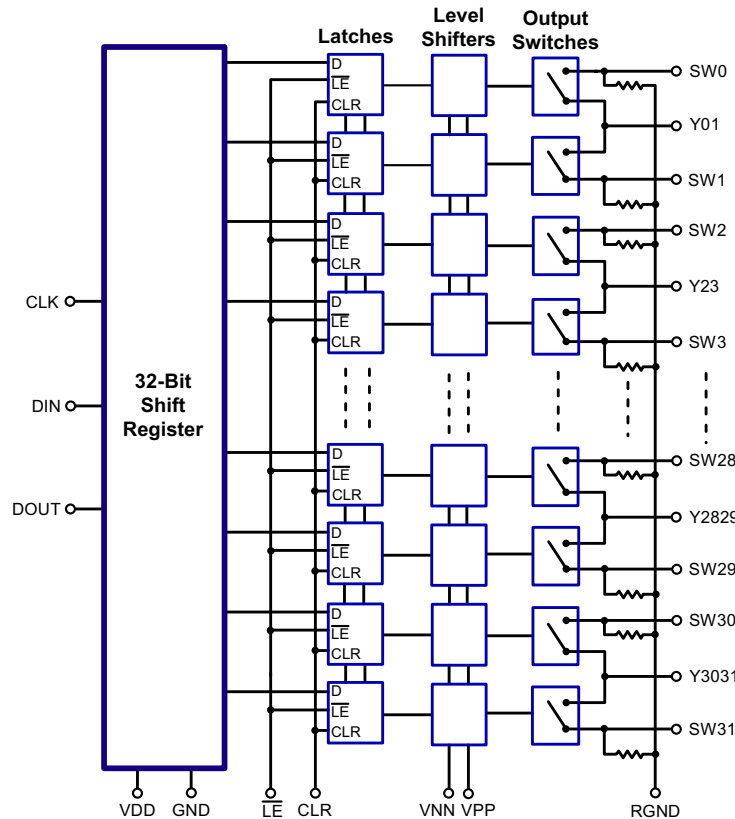
## General Description

The Supertex HV2901 is a low charge injection 32-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data are shifted into a 32-bit shift registers that can then be retained in a 32-bit latch. To reduce any possible clock feed through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V, and +160V/-40V.

## Block Diagram



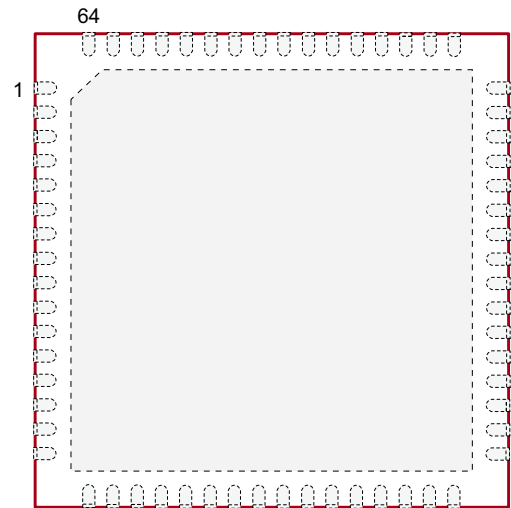
## Ordering Information

<b>Device</b>	<b>64-Lead QFN</b> 9.00x9.00mm body 1.00mm height (max) 0.50mm pitch
HV2901	HV2901K6-G

-G indicates package is RoHS compliant ("Green")

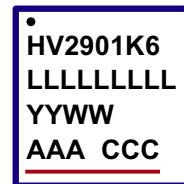


## Pin Configuration



**64-Lead QFN (K6)**  
(top view)

## Product Marking



L = Lot Number  
YY = Year Sealed  
WW = Week Sealed  
A = Assembler ID  
C = Country of Origin  
— = "Green" Packaging

Package may or may not include the following marks: Si or

**64-Lead QFN (K6)**

## Absolute Maximum Ratings

Parameter	Value
$V_{DD}$ logic supply	-0.5V to +6.5V
$V_{PP}$ - $V_{NN}$ differential supply	220V
$V_{PP}$ positive supply	-0.5V to $V_{NN}$ +200V
$V_{NN}$ negative supply	+0.5V to -200V
Logic input voltage	-0.5V to $V_{DD}$ +0.3V
Analog signal range	$V_{NN}$ to $V_{PP}$
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.5W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

## Recommended Operating Conditions

Sym	Parameter	Value
$V_{DD}$	Logic power supply voltage	3.0V to 5.5V
$V_{PP}$	Positive high voltage supply	+40V to $V_{NN}$ +200V
$V_{NN}$	Negative high voltage supply	-40V to -160V
$V_{IH}$	High level input voltage	$0.9V_{DD}$ to $V_{DD}$
$V_{IL}$	Low level input voltage	0V to $0.1V_{DD}$
$V_{SIG}$	Analog signal voltage peak-to-peak	$V_{NN}$ +10V to $V_{PP}$ -10V
$T_A$	Operating free air temperature	0°C to 70°C

### Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- $V_{SIG}$  must be  $V_{NN} \leq V_{SIG} \leq V_{PP}$  or floating during power up/down transition.
- Rise and fall times of power supplies  $V_{DD}$ ,  $V_{PP}$  and  $V_{NN}$  should not be less than 1.0msec.

## DC Electrical Characteristics (Over recommended operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	25	-	22	27	-	32		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -160V
		-	25	-	22	27	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	18	-	18	24	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -100V
		-	23	-	20	25	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V
		-	22	-	16	25	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -40V
ΔR <sub>ONS</sub>	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
R <sub>ONL</sub>	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 1A	
R <sub>INT</sub>	Value of output bleed resistor	-	-	20	35	50	-	-	KΩ	Output switch to R <sub>GND</sub> I <sub>RINT</sub> = 0.5mA	
I <sub>SOL</sub>	Switch OFF-leakage per switch	-	5.0	-	1.0	1.0	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V, V <sub>NN</sub> +10V	
V <sub>OS</sub>	DC offset switch OFF	-	300	-	100	300	-	300	mV	No load	
	DC offset switch ON	-	500	-	100	500	-	500			
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches OFF	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-			
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches ON, I <sub>SW</sub> = 5.0mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-			
I <sub>SW</sub>	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V <sub>SIG</sub> duty cycle < 0.1%	
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I <sub>PP</sub>	Average V <sub>PP</sub> supply current	-	16	-	-	20	-	22	mA	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
		-	14	-	-	14	-	14		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V	
I <sub>NN</sub>	Average V <sub>NN</sub> supply current	-	16	-	-	20	-	22	mA	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V	All output switches are turning ON and OFF at 50kHz with no load
		-	14	-	-	14	-	14		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
		-	14	-	-	14	-	14		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V	
I <sub>DD</sub>	Average V <sub>DD</sub> supply current	-	8.0	-	-	8.0	-	8.0	mA	f <sub>CLK</sub> = 5.0MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I <sub>SOR</sub>	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.7V	
I <sub>SINK</sub>	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

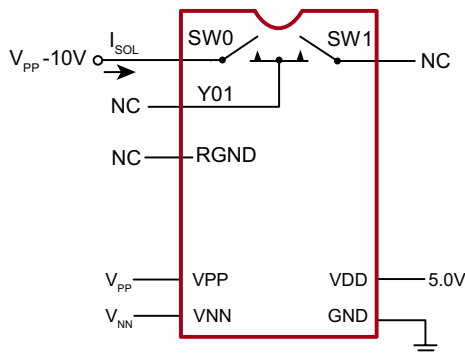
\* See Test Circuits on page 5

**AC Electrical Characteristics** (Over recommended operating conditions unless otherwise specified)

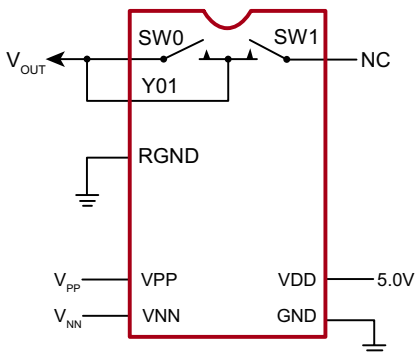
Sym	Parameter	0°C		+25°C			+70°C		Unit	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t <sub>SD</sub>	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t <sub>WLE</sub>	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	V <sub>DD</sub> = 3.0V
		12	-	-	12	-	12	-		V <sub>DD</sub> = 5.0V
t <sub>DO</sub>	Clock delay time to data out	25	100	25	78	100	25	100	ns	V <sub>DD</sub> = 3.0V
		15	40	15	30	40	15	40		V <sub>DD</sub> = 5.0V
t <sub>WCLR</sub>	Time width of CLR	55	-	55	-	-	55	-	ns	---
t <sub>SU</sub>	Set up time data to clock	21	-	21	-	-	21	-	ns	V <sub>DD</sub> = 3.0V
		7.0	-	7.0	-	-	7.0	-		V <sub>DD</sub> = 5.0V
t <sub>H</sub>	Hold time data from clock	5.0	-	5.0	-	-	5.0	-	ns	V <sub>DD</sub> = 3.0V
		7.0	-	7.0	-	-	7.0	-		V <sub>DD</sub> = 5.0V
f <sub>CLK</sub>	Clock frequency	-	8	-	-	8	-	8	MHz	V <sub>DD</sub> = 3.0V
		-	20	-	-	20	-	20		V <sub>DD</sub> = 5.0V
t <sub>R</sub> , t <sub>F</sub>	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t <sub>ON</sub>	Turn ON time	-	5.0	-	-	5.0	-	5.0	μs	V <sub>SIG</sub> = V <sub>PP</sub> -10V, R <sub>LOAD</sub> = 10kΩ
t <sub>OFF</sub>	Turn OFF time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V <sub>SIG</sub> slew rate	-	20	-	-	20	-	20	V/ns	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	20	-	-	20	-	20		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	20	-	-	20	-	20		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V
K <sub>O</sub>	OFF isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ/15pF load
		-58	-	-58	-60	-	-58	-		f = 5.0MHz, 50Ω load
K <sub>CR</sub>	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I <sub>ID</sub>	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
C <sub>SG(OFF)</sub>	OFF capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
C <sub>SG(ON)</sub>	ON capacitance SW to GND	25	50	25	38	50	25	50		
+V <sub>SPK</sub>	Output voltage spike SW	-	-	-	-	+150	-	-	mV	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
+V <sub>SPK</sub>		-	-	-	-	+150	-	-		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
+V <sub>SPK</sub>		-	-	-	-	+150	-	-		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
+V <sub>SPK</sub>	Output voltage spike Y	-	-	-	-	+150	-	-	mV	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
+V <sub>SPK</sub>		-	-	-	-	+150	-	-		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
+V <sub>SPK</sub>		-	-	-	-	+150	-	-		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V R <sub>LOAD</sub> = 50Ω
-V <sub>SPK</sub>		-	-	-	-	-150	-	-		
QC	Charge injection (per switch)	-	-	-	820	-	-	-	pC	V <sub>PP</sub> = +40V, V <sub>NN</sub> = -160V
		-	-	-	600	-	-	-		V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V
		-	-	-	350	-	-	-		V <sub>PP</sub> = +160V, V <sub>NN</sub> = -40V

\* See Test Circuits on page 5

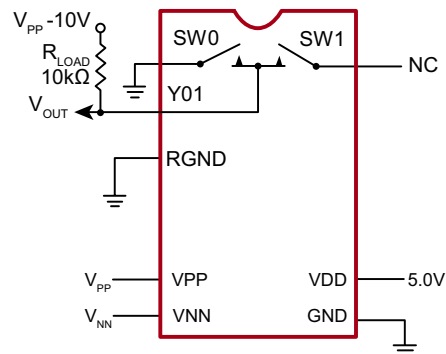
## Test Circuits



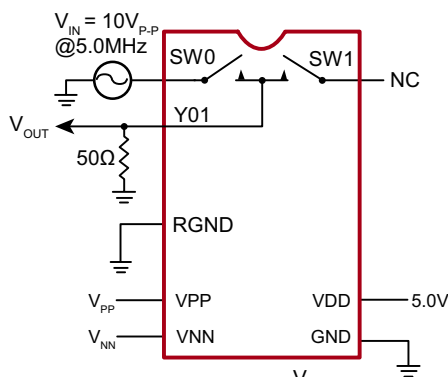
**Switch OFF Leakage**



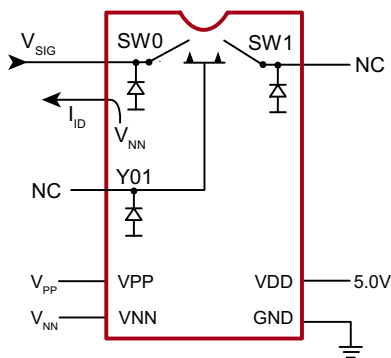
**DC Offset ON/OFF**



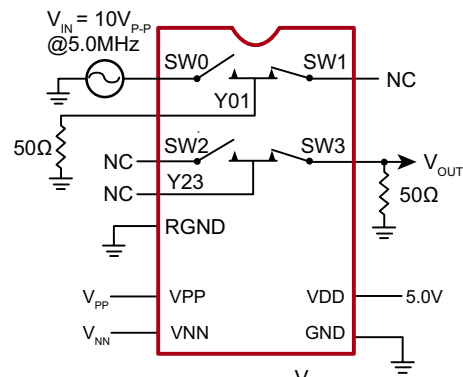
**T<sub>ON</sub>/T<sub>OFF</sub> Test Circuit**



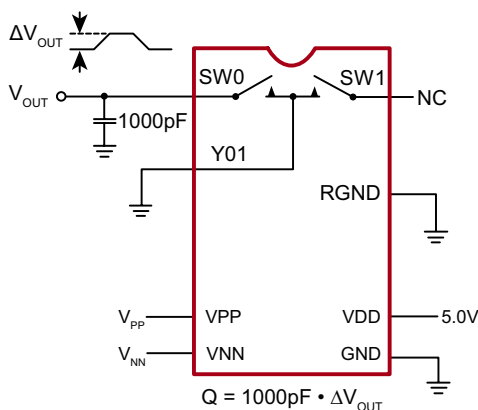
$K_o = 20 \log \frac{V_{OUT}}{V_{IN}}$   
**OFF Isolation**



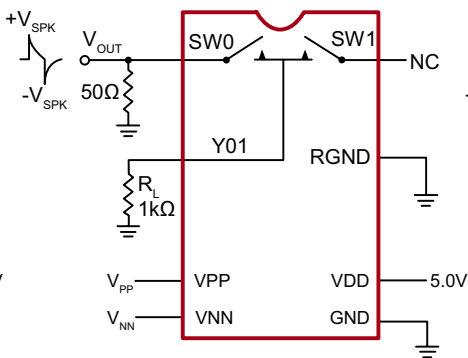
**Isolation Diode Current**



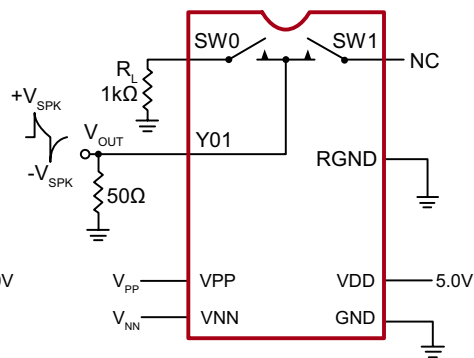
$K_{CR} = 20 \log \frac{V_{OUT}}{V_{IN}}$   
**Crosstalk**



$Q = 1000pF \cdot \Delta V_{OUT}$   
**Charge Injection**



**Output Voltage Spike SW**



**Output Voltage Spike Y**

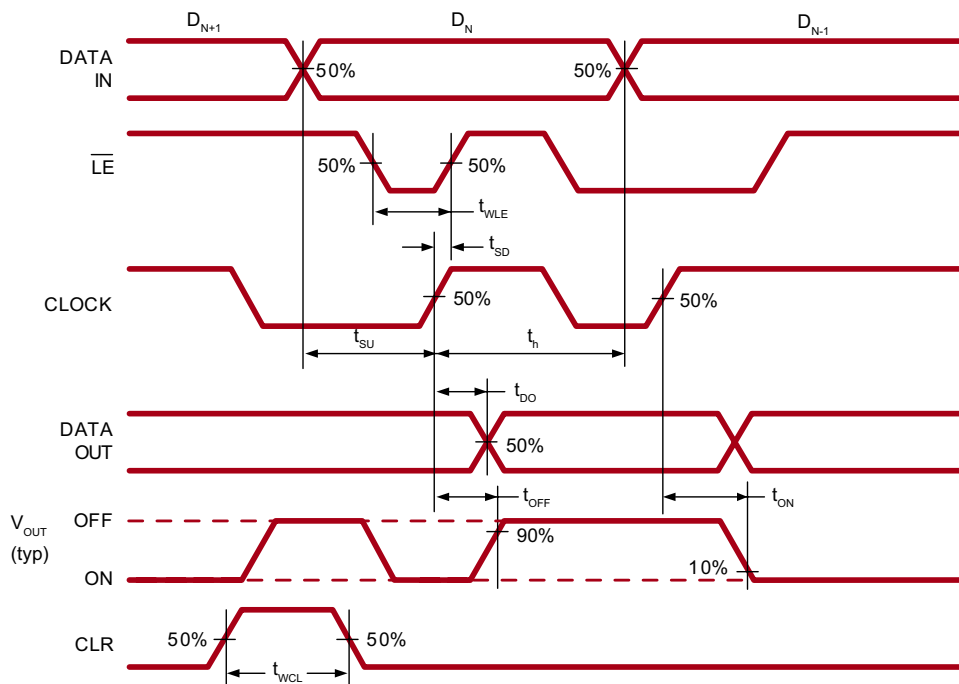
Truth Table

D0	D1	...	D15	D16	...	D31	$\overline{LE}$	CLR	SW0	SW1	...	SW15	SW16	...	SW31
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-		-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE					
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF					

Notes:

1. The 32 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 32 switches go to a state retaining their latched condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift registers data flow through the latch.
4.  $D_{OUT}$  is high when data in the register 31 is high.
5. Shift registers clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms



**Pin Function**

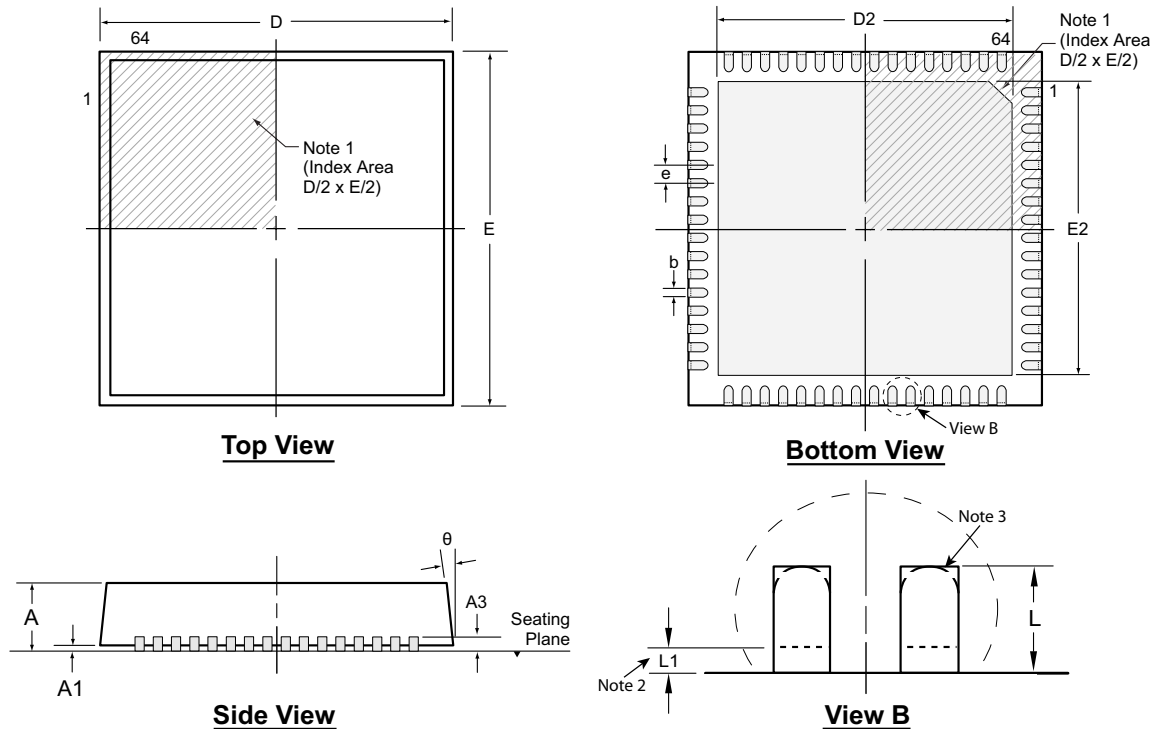
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	SW30	17	SW2	33	Y1213	49	SW19
2	Y3031	18	Y23	34	SW13	50	SW20
3	SW31	19	SW3	35	VPP	51	Y2021
4	NC	20	SW4	36	RGND	52	SW21
5	CLR	21	Y45	37	VNN	53	SW22
6	NC	22	SW5	38	SW14	54	Y2223
7	$\overline{LE}$	23	SW6	39	Y1415	55	SW23
8	CLK	24	Y67	40	SW15	56	SW24
9	VDD	25	SW7	41	SW16	57	Y2425
10	DIN	26	SW8	42	Y1617	58	SW25
11	GND	27	Y89	43	SW17	59	SW26
12	DOUT	28	SW9	44	VNN	60	Y2627
13	NC	29	SW10	45	RGND	61	SW27
14	SW0	30	Y1011	46	VPP	62	SW28
15	Y01	31	SW11	47	SW18	63	Y2829
16	SW1	32	SW12	48	Y1819	64	SW29

VSUB (Thermal Pad)	The central thermal pad on the bottom of package must be connected to VNN externally
--------------------	--

# 64-Lead QFN Package Outline (K6)

9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.20	8.90	7.60	8.90	7.60	0.50 BSC	0.30	0.00	0°
	NOM	0.85	0.02		0.25	9.00	7.70	9.00	7.70		0.40	-	-
	MAX	0.90	0.05		0.30	9.10	7.80	9.10	7.80		0.50	0.15	14°

Drawings are not to scale.

Supertex Doc.#: DSPD-64QFNK69X9P050, Version B020112

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

**Supertex inc.** does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)