HVCMOS Drivers for Non-Impact Printing

This article discusses the use of monolithic high voltage ICs for non-impact printing and plotting applications. Supertex's HVCMOS® process technology allows combining low voltage logic as well as high voltage DMOS outputs up to 400V on one monolithic IC. The principle of operation for inkjet and electrostatic printing/plotting is also described briefly.

Inkjet Printing

The inkjet printing industry has grown dramatically in recent years because of the low cost and improved quality. There are two basic types of inkjet printing technologies: Continuous and Drop-on-Demand, though there are several variations. Both systems, under electronic digital control, "paint" the images on a substrate using carefully formulated and controlled jet droplets. The continuous method in Figure 1 directs the flight of charged ink droplets to the receptor substrate, e.g., paper.

In the drop-on-demand method, however, ink droplets are ejected from the nozzle only as required; no circulation system is needed. Figure 2 shows a drop-on-demand inkjet printing method. The expulsion of droplets from the nozzle is controlled by an internal change in pressure caused by a piezoelectric transducer.

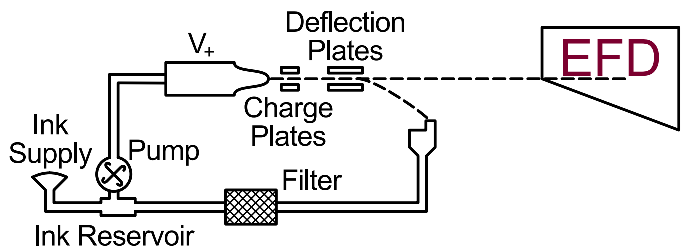

Figure 1: Continuous Method

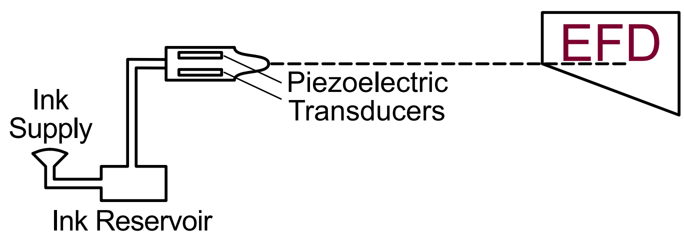

Figure 2: Drop-on-Demand

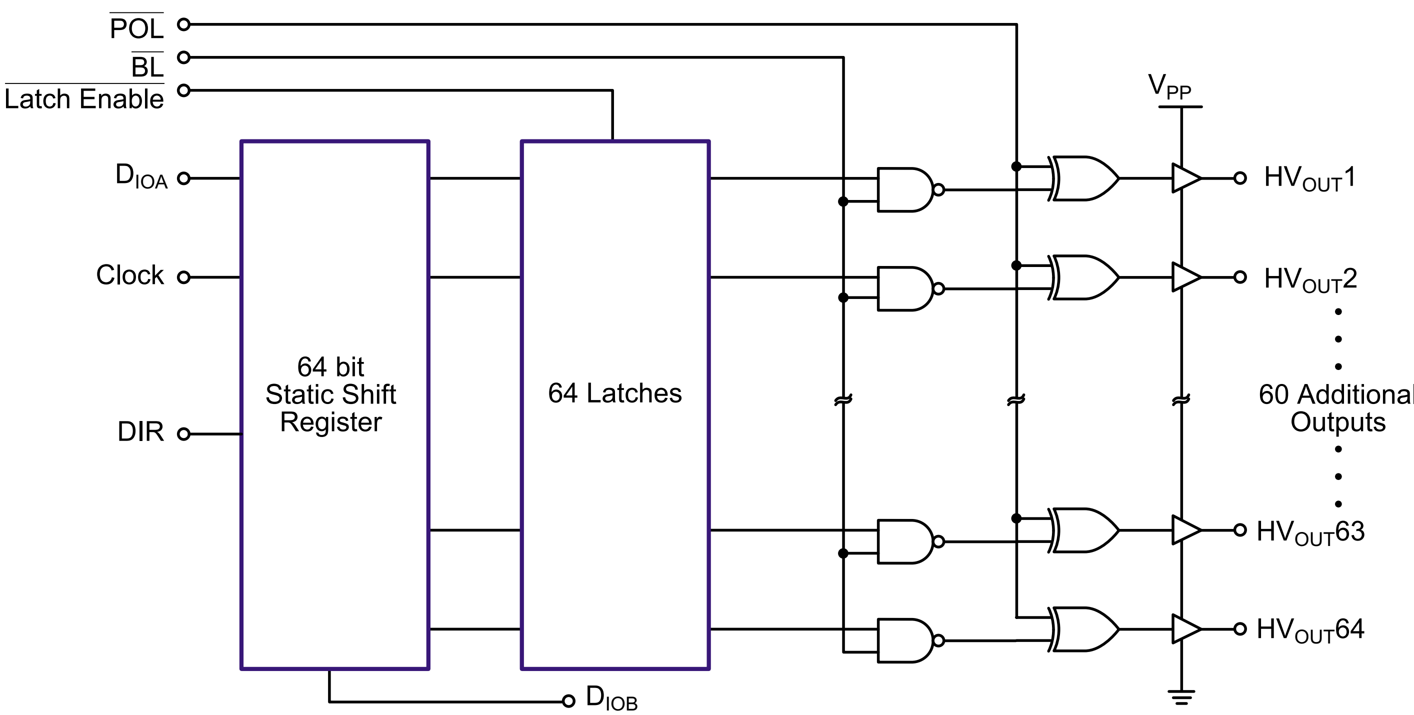

Figure 3: HV34 Functional Block

High Voltage Drivers for Inkjet Printers

Supertex HV34, which was designed for driving the deflection plates to control the path of charged ink particles, can help optimize performance and cost of inkjet printers.

The HV34 is a low voltage serial input to high voltage parallel output converter with 64 push-pull outputs at up to 180V. Figure 3 shows a functional block diagram of the HV34. This device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of the data shift through the device. Data output buffers are provided for cascading multiple devices. The low voltage logic section of the HV34 can be operated either at a 5.0 or 12V logic supply voltage. The corresponding maximum data shift frequency possible with these logic supply voltages is 6.0 or 12MHz respectively. The user can therefore choose the appropriate V_{DD} voltage to suit the application requirements.

Normally, the load on the outputs of the drivers is capacitive. Since the output has a true complementary MOS configuration, either the P-channel or N-channel MOSFET can be turned on at a time. When the output P-channel FET is turned on, the capacitive load starts to charge and its voltage increases until it reaches V_{PP}.

One can calculate how fast a certain value of the capacitive load can be charged up, as explained in the following example. Assuming the voltage on the load is at zero volt and a DC voltage of 100V is applied to the V_{PP} terminal of the IC. As soon as the P-channel transistor turns on, the load starts to charge up. Initially, the drain-to-source voltage is at maximum value, because V_{OUT} = 0V and $V_{DS} = V_{PP} – V_{OUT}$. This P-channel transistor operates in saturation and delivers maximum possible current to charge the capacitor. The dV/dt is calculated as:

$$dV/dt = I/C$$

where I is the source current of the P-channel transistor and C is the load capacitance. Assuming a capacitive load of 1.0nF, the output source current of the HV34 is 5.0mA, so the dV/dt is:

$$dV/dt = I/C = 5 \times 10^{-3}/1 \times 10^{-9} = 5V/\mu s$$

Since the V_{PP} is at 100V, the time required to charge the load to 90% of the V_{PP} is $90\%V_{PP}$/(dV/dt) = 18µs. The dV/dt to charge the load for the remaining 10% of the V_{PP} will be slower. This is due to decrease in the V_{DS} voltage of the P-channel transistor as the voltage on the load increases. The transistor finally gets out of saturation and operates in the linear region, thereby causing a reduction in the output current.

In the above example, the output of the IC was “hot switched.” The term “hot switch” means that a high voltage DC supply is applied to device V_{PP} at all times even when the high voltage outputs are being switched. On the other hand, “cold switch” means that the high voltage supply is brought to a much lower voltage, sometimes to zero volts depending on the application, while the high voltage outputs are being switched. After switching the outputs, the high voltage supply is brought up to the desired voltage level.

Cold switching may be necessary on some ICs as this prevents possible damage to the device due to large crossover current during transition from the high-side transistor to the low-side transistor and vice versa. In a hot switching system, only a DC high voltage power supply is needed; this is simpler than the cold switch system where an extra high voltage switch or a high voltage ramp circuit is necessary.

When the load connected to the output of the IC is very large, the risk of damage to the output transistors is not only from the crossover current but also because the safe operating area of the device may be exceeded. This risk is eliminated by ramping the V_{PP} which minimizes the drain-to-source voltage drop across the device by controlling the slew rate of the ramping voltage. Ramped high voltage supplies are not only less strenuous to the output of the ICs, but have the following additional advantages:

1. *Lower power dissipation in the high voltage IC.*
2. *Reduced switching noise, which has several disadvantages, e.g., malfunction of logic, latch-up, etc.*

The rise and fall time of the output voltage is determined by the output sink and source current of the device and the size of the load. The slew rate of ramp voltage can be designed to closely follow the rising load voltage to minimize the drain-to-source voltage drop. Figure 4 shows a typical ramp generator circuit.

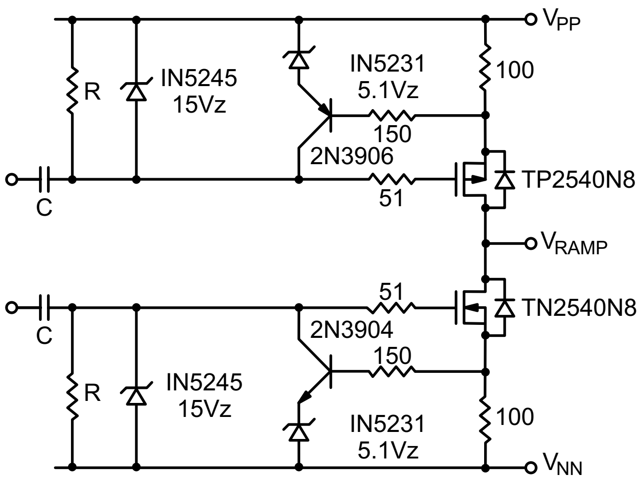

Figure 4: Ramp Generator

The above circuit utilizes Supertex high voltage DMOS transistors TP2540N8 and TN2540N8. The 15V zener diodes provide extra protection for the gate of the DMOS transistors. The value of the R and C is chosen in such a way that the time constant of this RC is much greater than the output pulse width of the ramp generator. V_{NN} and V_{PP} are fixed voltages available from the system's main power supply. If a negative voltage is not needed, the V_{NN} can be kept at zero volt.

The input A and B are connected to 5.0V or 12V logic IC outputs. Care must be taken to ensure that either TP2540N8 or TN2540N8 is on at a time to avoid large crossover currents flowing through both transistors at the same time, which may cause catastrophic failure.

In applications where different V_{PP} voltages are required to be applied to the deflection plates, a Supertex HV20220PJ can be used to connect the V_{PP} pin of the IC to the appropriate high voltage. Figure 5 shows the block diagram of HV20220PJ, which is used to supply 4 different voltages to the V_{PP} of the HV34 by controlling the SW0, SW1, SW2 and SW3 turned-on time.

Piezoelectric transducers can also be driven by Supertex high voltage push-pull drivers. The high voltage output of the driver forces the interspace of the piezoelectric transducer to expand, thereby sucking liquid ink into the nozzle. Then, when a high voltage of reverse polarity is applied to the transducer while the nozzle is filled with ink, the ink will be expelled and deposited on the paper.

Electrostatic Printing/Plotting

Electrostatic printers and plotters produce images by converting vector data into raster data and applying dots to the medium. This allows them to pay down the image across the entire width of the media simultaneously and thus increase printing speed.

The electrostatic printing/plotting process typically uses a toner and a paper that will hold charge. The paper is passed over the print head, which contains a stylus array (NIB) that lays down negative charges on the paper. The higher the charge voltage across the paper (i.e., between the print head NIB and SHOE), the better the image definition.

To implement electrostatic printing technology requires very high-voltage driver circuits for the stylus arrays as shown in Figure 10. The current required, however, is relatively low, typically below 1.0mA.

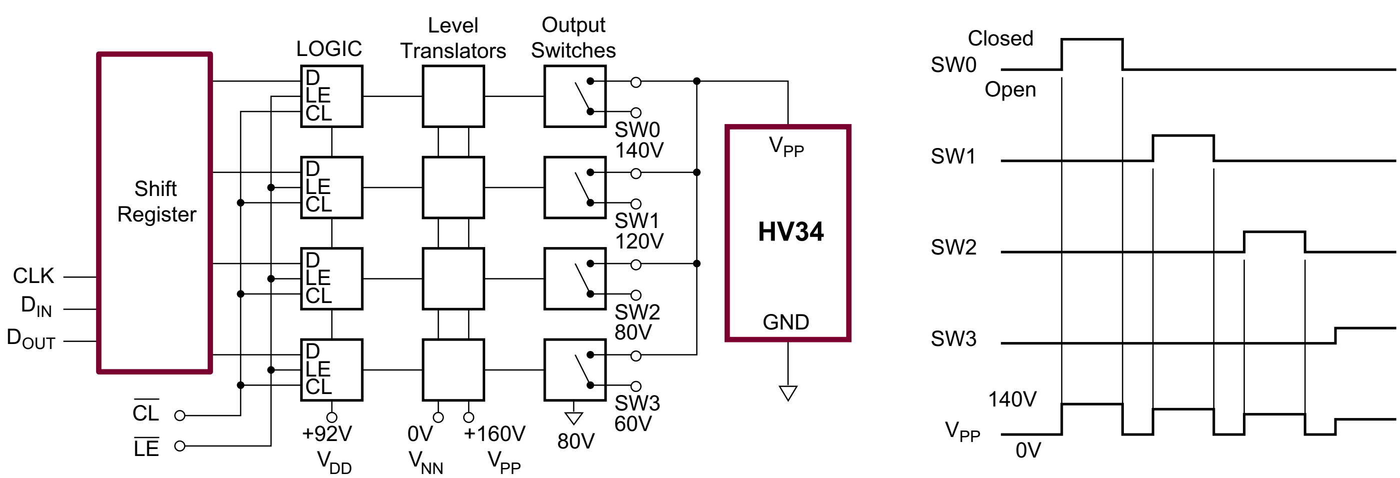

Figure 5: HV20220PJ for Selecting V_{PP} Voltages

HV507

The HV507 is a low voltage serial input to high voltage parallel output converter with 64 push-pull outputs with a 300V rating. Figure 11 shows a functional block diagram of the HV507. This device consists of a 64 bit shift register, 64 latches and logic control to perform the output enable and polarity functions. A direction (DIR) pin controls the data shift through the device, which can be clockwise or counterclockwise as desired. Since many devices are often used in one system, data output buffers are provided for cascading purposes.

The HV507 allows up to 8.0MHz data shift frequency with logic supply voltage of 5.0 volts, which is convenient to interface with microcomputers directly without the need for voltage shifting circuits.

Since a very high voltage is used for electrostatic printers and plotters, arcing can occur between the NIB or stylus and the SHOE due to the pin holes or cracks in he paper. High current during this arcing will be destructive to the driver IC, and adding circuitry duration is afforded by the saturation current of the HV507, which typically is less than 1mA. However this is really not adequate because considerable heat may be generated for durations longer than a few milliseconds. Current limiting resistors are required to lower the current further.

High Voltage Drivers for Piezos HV45 & HV55

The Supertex HV55 and HV45 are ideally suited for high current piezo applications. Piezo applications can cover a wide variety of mechanical movement applications, these include inkjet printers, flow control valves, micro-machines, and weaving machines.

The HV55 is a low voltage serial input to high voltage parallel output converter with 32 N-channel open-drain outputs with a 300V rating. Figure 8 shows a functional block diagram of the HV55. This device consists of a 32 bit shift register, 32 latches and logic control to perform the output enable and polarity functions. Since many devices are often used in one system, data output buffers are provided for cascading purposes.

The HV55 allows up to 8.0Mhz data shift frequency with logic supply voltage of 12 volts.

The HV45 is a high voltage open-drain P-channel device that can be operated up to -300V. The functional block diagram of the HV45 is the same as for HV55 except that the output section consists of open drain P-channel MOSFETs. Being a P-channel device, the polarity of all the voltages are reversed.

For high performance systems, a 300V push-pull configuration can be formed using the combination of the HV55 and HV45 (Figure 7). In this configuration, level shifting of the logic signal is required because the input logic voltages for both the HV55 and HV45 are referenced to V_{SS}. The circuit shown in Figure 9, utilizing opto-couplers, may be used to achieve the desired level shifting and isolation.

Assume that the logic input signals coming from the TTL logic to the opto-couplers are 0 to 5V. The power needed to run the opto-couplers is taken from the two floating power supplies. The logic signals coming out of the opto-couplers are referenced to the floating power supplies. The V_{SS} voltage normally is ramped, as discussed earlier, to minimize the

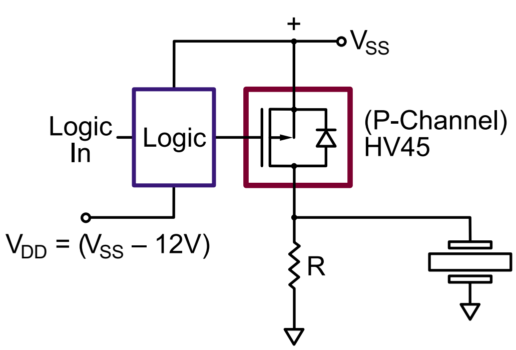

Figure 6: Electrostatic Printing/Plotting Open Drain Configuration

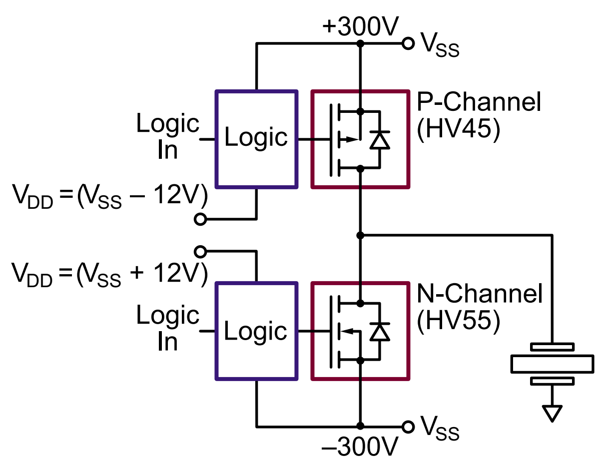

Figure 7: Electrostatic Printing/Plotting Push-Pull Configuration

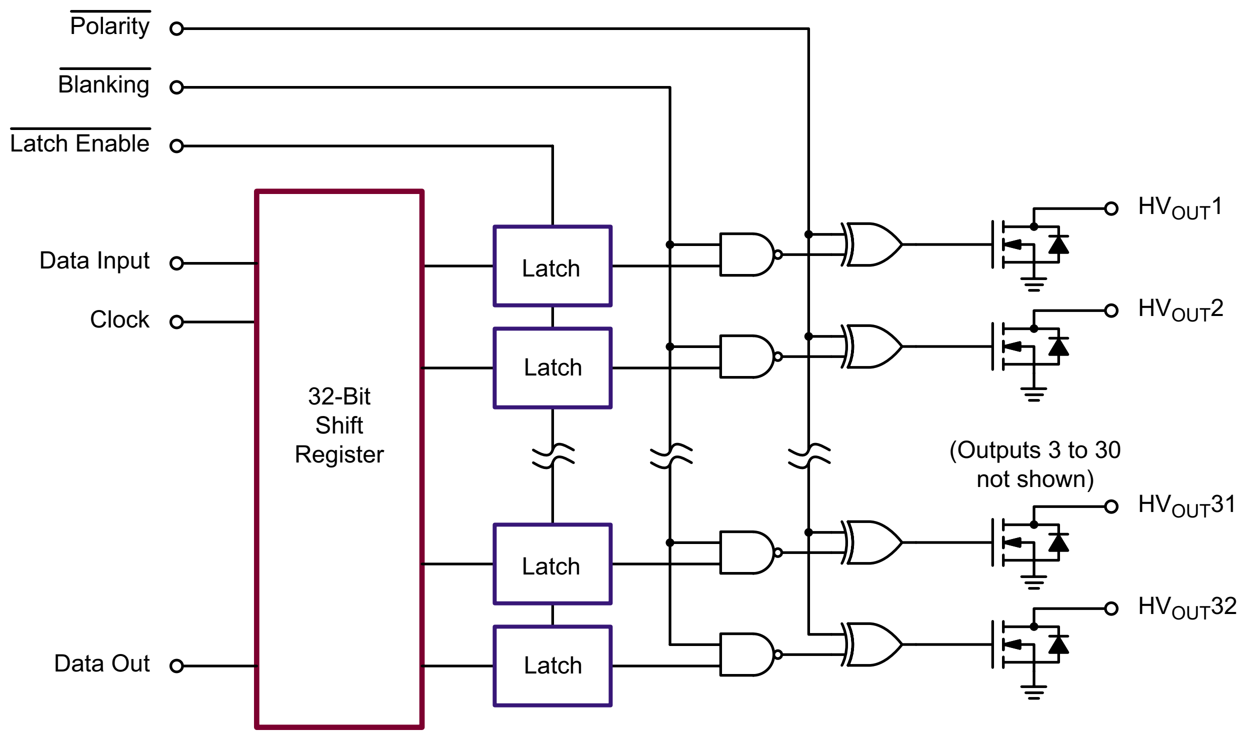

Figure 8: HV31 Functional Block

voltage drop across the output transistor of the device. The two floating power supplies are formed by using a transformer, the primary winding of which is connected to the 120V AC utility power line. There are two secondary windings on the transformer; the outputs will be rectified by the bridge rectifiers and stabilized by LM340 linear regulators.

Since a very high voltage can be used for piezos, shorting can occur between the output and ground due to breakdown of the crystal. High current during the short can be destructive to the driver IC, and adding circuitry for protection becomes necessary. Current limiting resistors are required to provide output short circuit protection because these devices can easily provide more than 60mA source and 100mA sink current per output.

Electrostatic Printing/Plotting

The electrostatic method of printing/plotting is relatively new. Electrostatic printers and plotters produce images by converting vector data into raster data and applying dots to the medium. This allows them to lay down the image across the entire width of the media simultaneously and thus increase printing speed.

The electrostatic printing/plotting process typically uses a toner and a paper that will hold charge. The paper is passed over the print head which contains a stylus array (NIB) that lays down negative charges on the paper. The higher the charge voltage across the paper (i.e., between the print head NIB and the SHOE), the better the image definition.

To implement electrostatic printing technology requires very high-voltage driver circuits for the stylus arrays either in an open drain configuration as shown in Figure 6 or, preferably in a push-pull configuration for better efficiency as shown in Figure 7. The current required, however, is relatively low, typically below 1mA.

Conclusion

Multichannel high voltage ICs provide practical solutions for driving printer/plotter heads utilizing inkjet and electrostatic technologies. High density solutions, which require a low unit area per output channel, save printed circuit board space and costs. The high voltage devices mentioned in this application note are also available in die form suitable for mounting the chips on circuit boards or “flip chip” on suitable substrates.

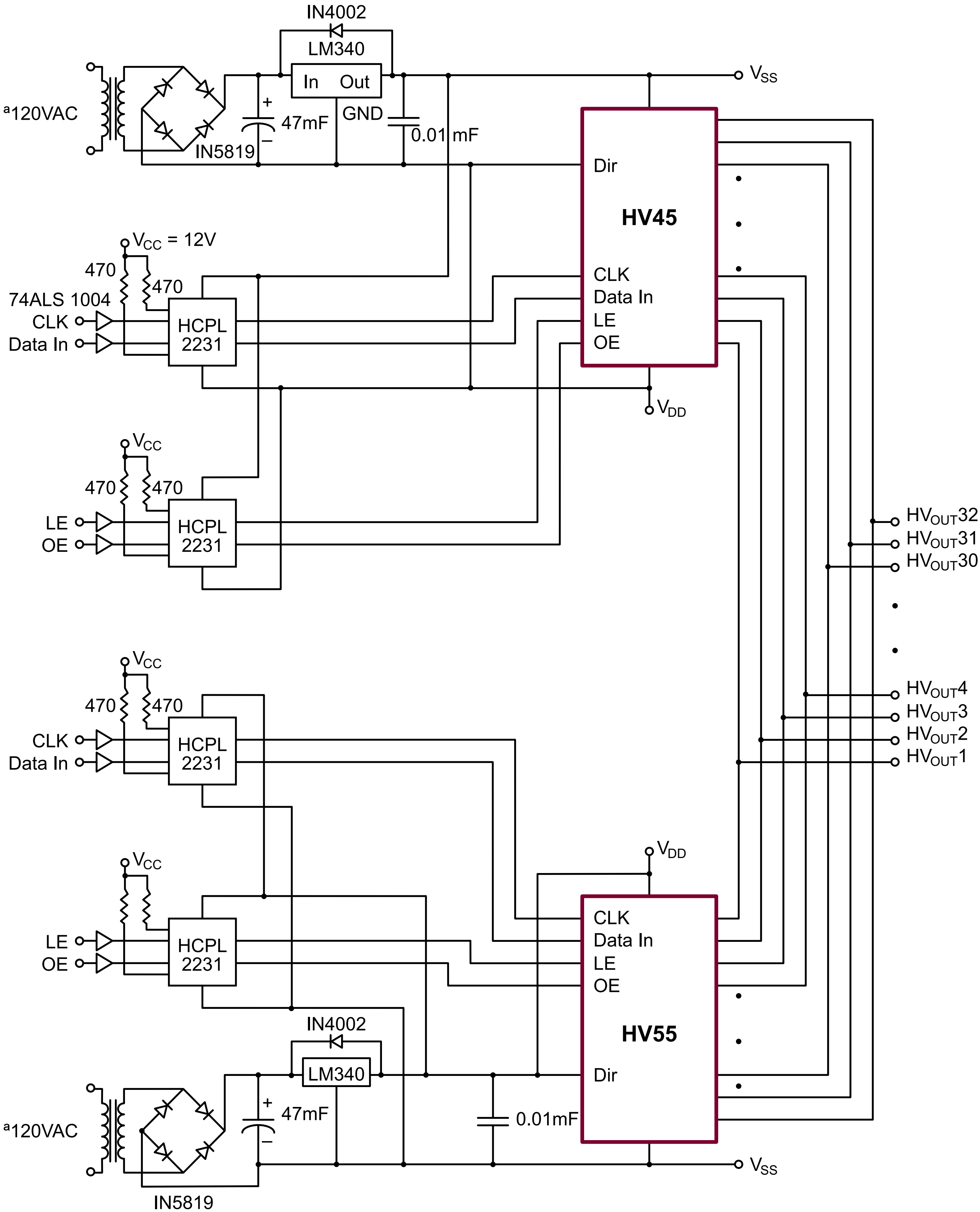

Figure 9: Level Translation Using Opto-couplers

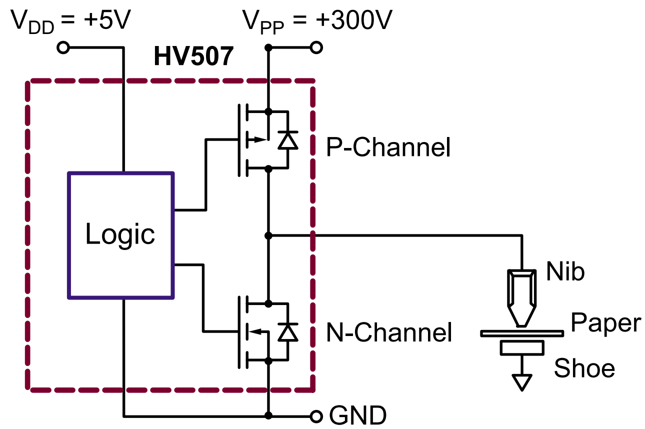

Figure 10: Electrostatic Printing/Plotting Push-Pull Configuration

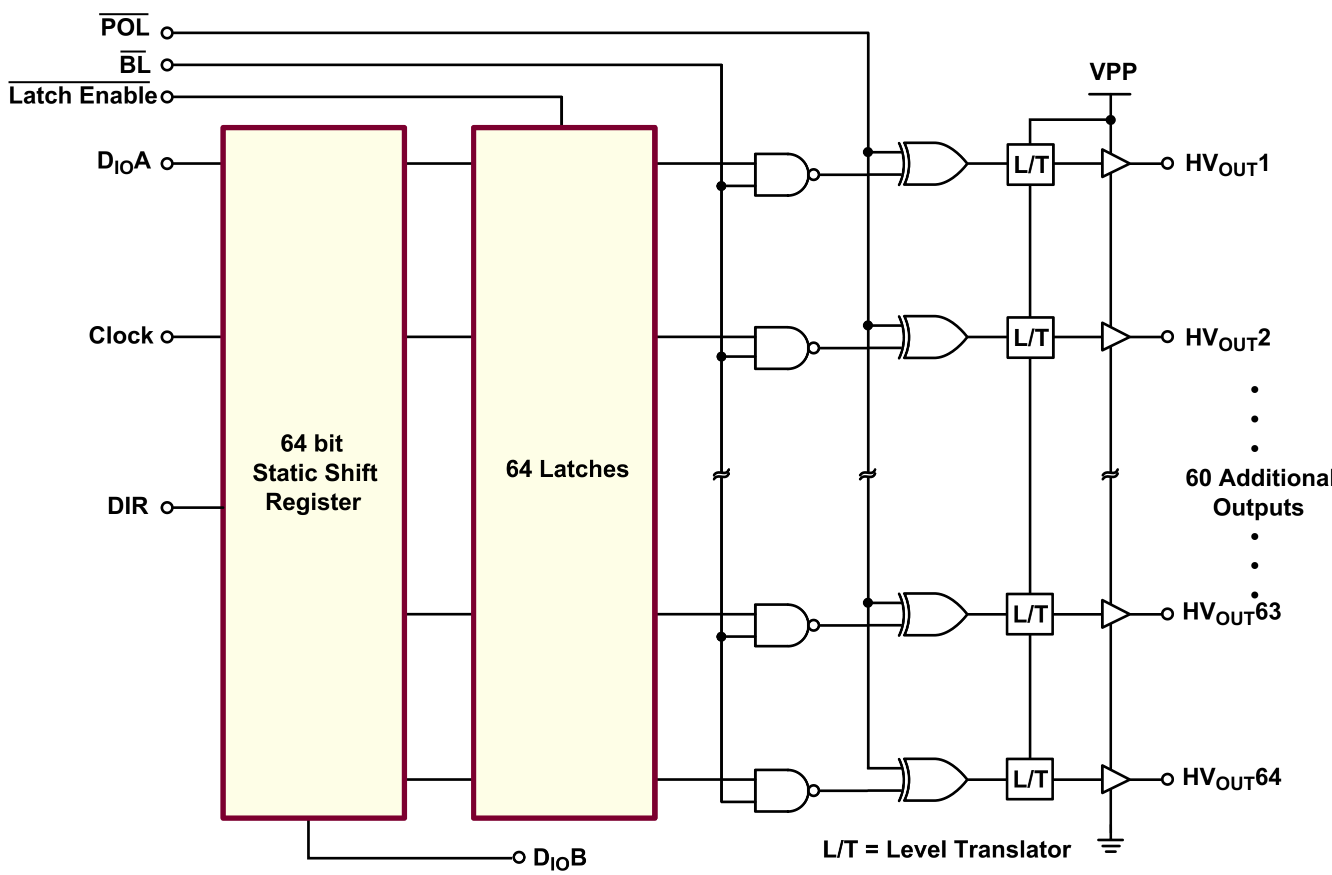

Figure 11: HV507 Functional Block Drawing

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